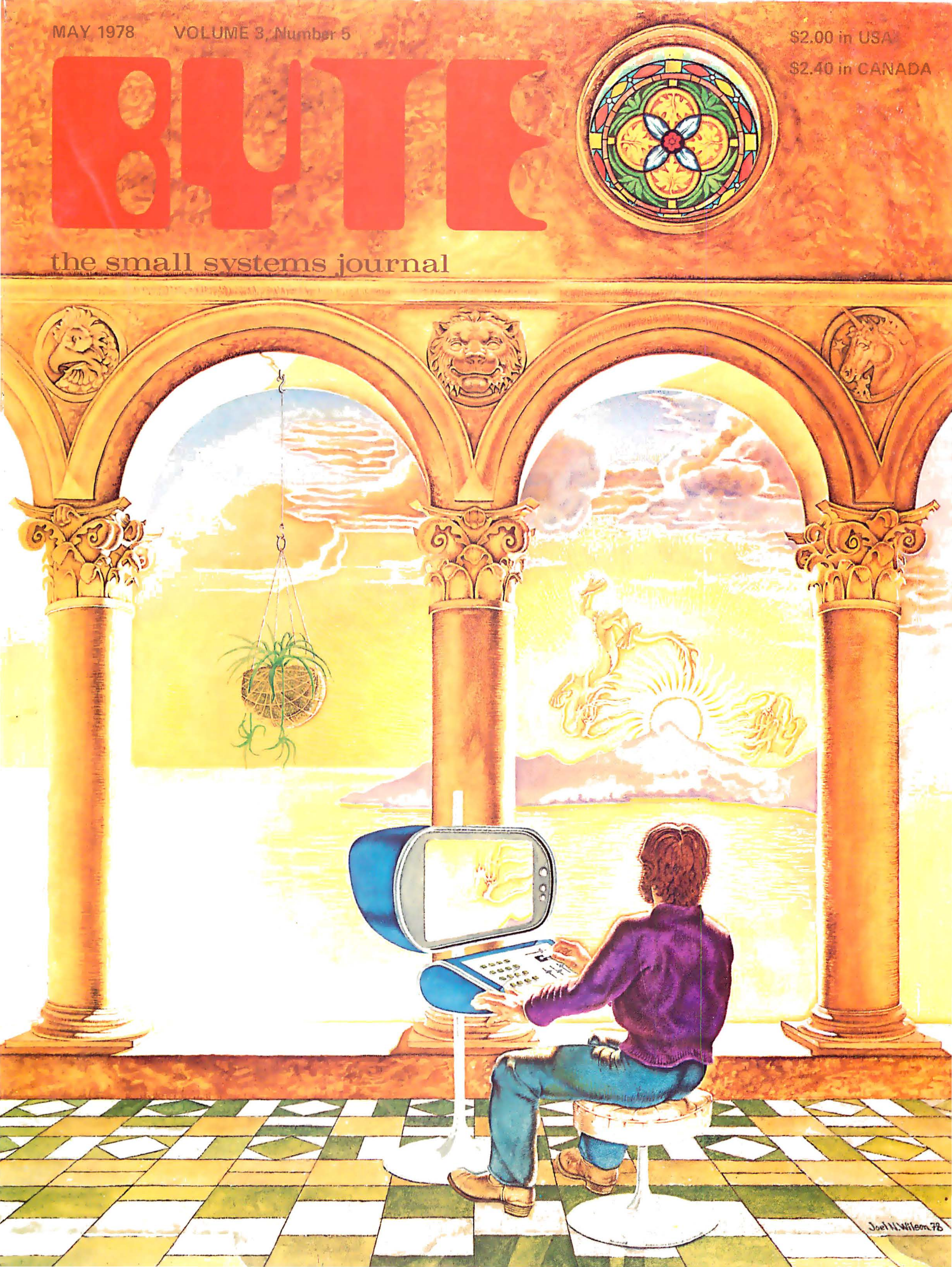

MAY 1978 VOLUME 3, Number 5
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BYTE
the small systems journal
Joel N. Wilson 78

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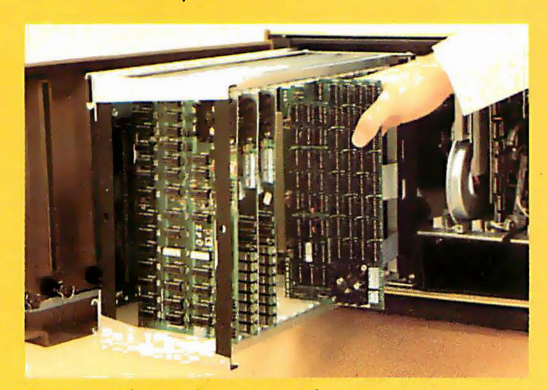


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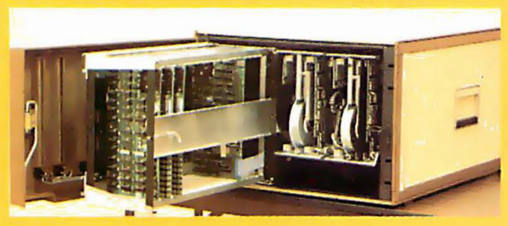
MORE ABOUT THE SYSTEM THREE . . .



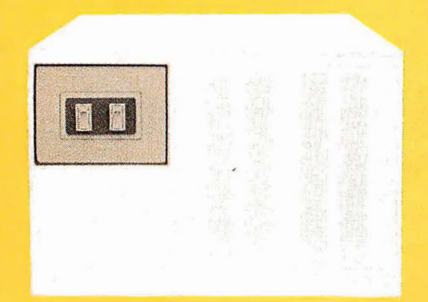
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Volume 3 Number 5

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In This BYTE

About the Cover:

The computer experimenter of the future shown on this month's cover is using a computer graphics terminal created by artist Joel N Wilson to make a point: computer graphics has come of age. Future scenes such as Joel's painting are not far off, and this month's issue is largely devoted to the fascinating world of computer graphics.

Taking photographs of your video display is an inexpensive alternative to buying a printer or other hard copy device for your computer. However, it's not always as easy as it sounds. Dr Dwight D Egbert gives some valuable tips on the subject in The Photograph Is Also a Hard Copy. *page 10*

Real 3-D graphics? It sounds like an impossible concept, even given the magic of minicomputers, but that is just what authors Timothy Walters and William Harris have created. Read Graphics in Depth: 3-D Adds a New Dimension to Your Display and find out how to create images that change perspective as you vary your viewing angle. *page 16*

What's the difference between an RF monitor and a direct video entry monitor? Find out in Convert Your TV Set to a Video Monitor. Dan Fylstra explains the relative merits of the two approaches to video displays, and gives you some idea of the techniques necessary to implement both methods. *page 22*

Would you like to try some pseudocolor? How about an 8 level grey scale? High density video graphics is an exciting application of personal computing. There are many video display boards on the market to help you get started. Read about one of them in The Matrox ALT-256 Video Board, by Gary Ruple. *page 24*



page 32

Color graphics is an exciting branch of personal computing. Ordinary video display programs take on a new luster when converted to color. Authors Thomas A Dwyer and Margot Critchfield discuss the use of Color Graphics on the Compucolor 8051. *page 32*

Is there a practical microcomputer PASCAL language system? Ken Bowles, of the Institute for Information Systems at the University of California San Diego, outlines what is perhaps one of the most significant software developments of the past year or so: the UCSD PASCAL system now available for LSI-11, 8080 and Z-80 machines and soon to be available for other major general purpose microcomputer systems. Read Ken's account of UCSD PASCAL: A (Nearly) Machine Independent Software System. *page 46*

A hidden line subroutine for your plotter can make the difference between an average plot and a professional looking one. The algorithms aren't as difficult as you might think. Read Hidden Line Subroutines for Three-Dimensional Plotting by Mark Gottlieb and find out more. *page 49*

One way to learn more about display systems for television is to read a detailed description of a practical video driver program. John Webster and John Young have done just that in GRAPH: A System for Television Graphics. In part 1, this month, the authors provide background information and begin a detail discussion of this character editing system used for titling and graphics associated with educational videotape production. *page 62*

Did you ever wish your video display could handle Greek letters, subscripts, different size fonts, or even APL characters? How about special graphics characters? Find out how to add these and many other characters to your video display system in A Programmable Character Generator by Larry Weinstein. *page 79*

When designing a light wand and signal processor it is desirable to have as few external variables as possible affecting the output. In A Low Cost Light Wand Amplifier, Robin C Moseley examines some of the variables that must be considered and describes a particular signal processor which is tolerant of many external variables. *page 92*

Last month Steve Ciarcia described the transmitter section of his AC wireless remote control system. This month read the concluding description of the receiver in Tune In and Turn On, Part 2, and start experimenting with your own computer controlled wireless appliance and light control system. *page 97*

This month, Jack Bryant and Manot Swasdee complete their description of How to Multiply in a Wet Climate with the details of multiplier hardware and a program to test the multiplier in comparison with an equivalent software multiplication. *page 104*

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Processor Technology

Editorial

On the Uses of Snowstorms in Computer Science

By Carl Helmers

By the time you read this, the events of this past week will be history as the seasons progress. Monday evening (Feb 6) it began to snow a bit in Peterborough. It had apparently been snowing through most of the day at places further south along the eastern seaboard, but I had no expectation of anything out of the ordinary. After all, the morning news and weather reports I listened to had said we might get a foot of snow, but that is hardly unusual. One of the reasons for locating one's home and place of business in the hills of New Hampshire is to take advantage of those opportunities for transient beauty which are presented each year by a full cycle of seasons. All six seasons — Summer, Foliage, Winter, Mud, Spring and Black Fly — come and go in a regular cycle each year. Since the first week of February is solidly within the Winter phase of the cycle, another snowstorm is not a major event.

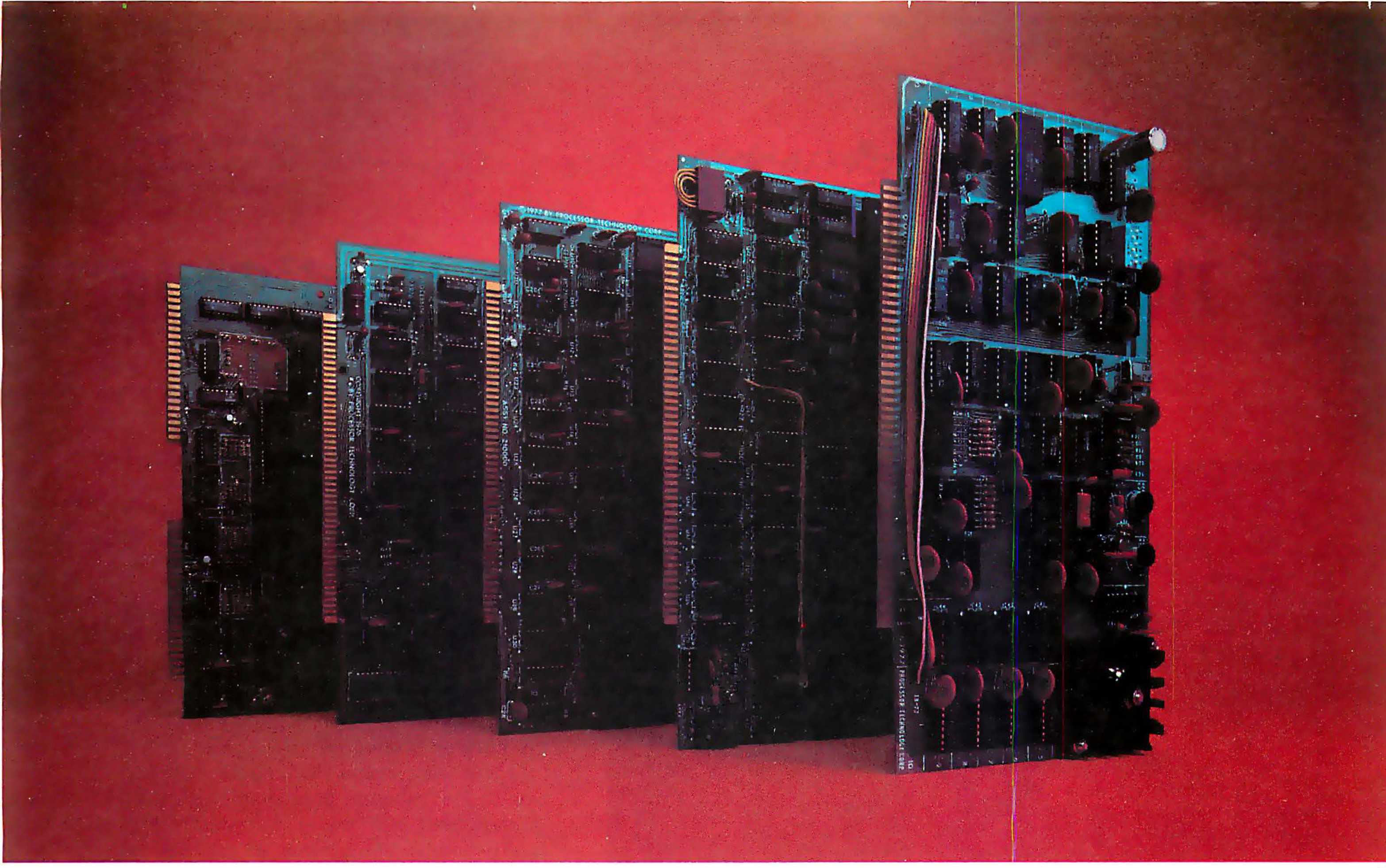
The beautiful clear day full of sunshine which is this present Wednesday certainly speaks well of the climate. But in between Monday and Wednesday was that equally natural event which was a winter's gale, or "Nor'easter" as this type of storm is called by the local people. Already, the people responsible for writing instant history books have started calling the weather conditions yesterday by the name "The Great Blizzard of '78." The pundits of course were not particularly original, for a very similar term is often applied to a storm of approximately 90 years earlier in 1888. And the pundits also show a particular regional bias. I don't recall any special terms of endearment applied to the storm which a half a week earlier had given New England torrential rains while the Midwest was racked with almost equivalent snows and hurricane like winds. But somehow, if a large amount of snow becomes your own provincial local problem in Philadelphia, New York, Providence or Boston, it becomes "*The* Blizzard of '78," ayup. Very simply, what happened was that a capricious storm decided to sit on Cape Cod for most of Tuesday, channelling water laden air off the

Continued on page 135

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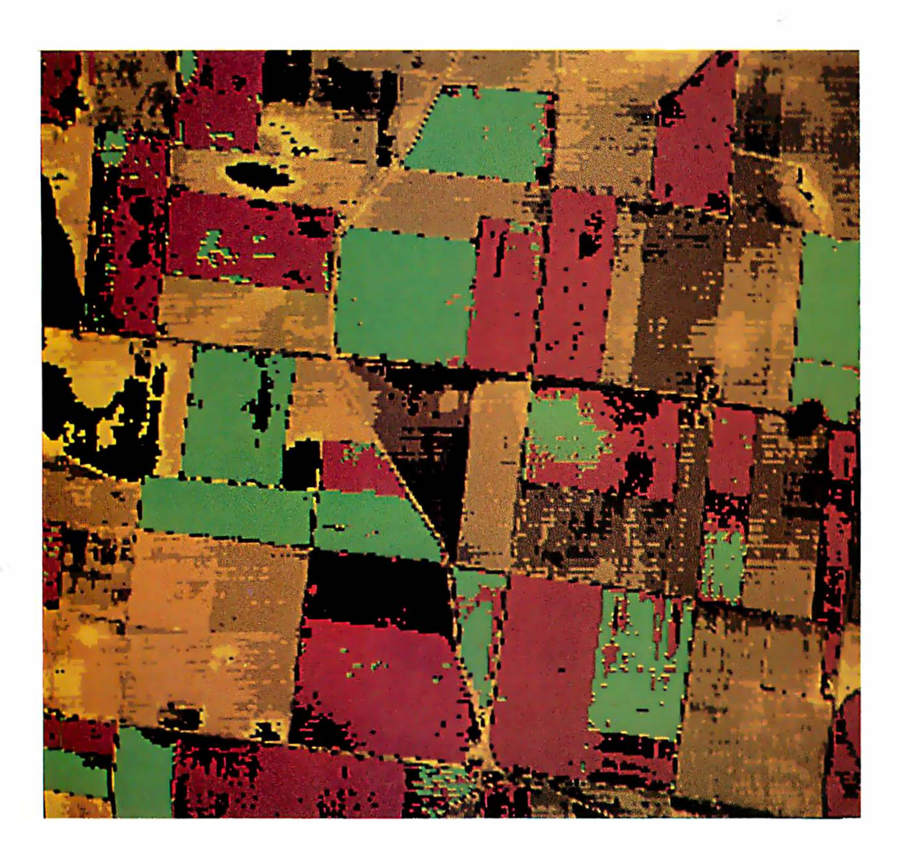


Photo 1.

Even with the arrival of low cost alphanumeric printers for hobby computers, there are still several situations in which photographs from video displays are the most satisfactory form of hard copy. This is particularly true when you are displaying graphs or image data in black and white, or with almost any color display. In fact, most professionals working with color displays are still forced to photograph their video displays to obtain color hard copy. At present, satisfactory color hard copy devices range in price from $50,000 to well over $500,000.

Likewise, the current small system printers are not suitable for image data, whether black and white or color. Image data differs from the usual alphanumeric and graphics data because the display is no longer binary (black or white, color or no color). Instead, image data is displayed in a two-dimensional array or raster, and each element of the array or each picture element (pixel) can possess one of several grey levels or colors. In the field of personal computing, the Cromemco Dazzler is capable of displaying image data in up to a 64 by 64 pixel array with each pixel one of 16 possible grey levels or 15 possible colors. The Apple II has a similar mode of operation with 16 colors and black available in a 44 high by 40 wide array. For these types of displays it will probably be many years before a viable alternative to photography exists for low cost hard copy.

There are several techniques you can employ to produce photographs of video displays that will insure consistently high quality results. Many kinds of cameras can be used with these techniques, but by far the easiest to use is the single lens reflex. Some models of Polaroid cameras equipped with close-up attachments also work well.

Whichever camera you use, it is essential that you attach it to a solid mount. This might be a tripod, a low cost camera clamp, or a device of your own construction. The camera should be positioned perpendicular to the video display screen so that the screen is centered and almost completely fills the viewfinder. As with most of the techniques discussed here, consistency is paramount if you want to obtain reliable and repeatable results. To achieve consistency in camera positioning, it is desirable to build some simple mechanism to hold the camera in the same location every time you use it. Alternatively, if you use a tripod, mark the leg positions on the floor with tape, or at least measure the distance from the screen to the camera with a tape measure.

Once the camera is mounted, the room lights should be dimmed or preferably turned off when you actually take a picture. If the room contains windows, pull the shades or completely block them. You will obtain the best results in a completely dark room. If you cannot completely eliminate light from the room, position the display so that any light sources are behind it to prevent light reflections from the screen. Make a habit of observing any such reflections while looking through the camera viewfinder. Normally, reflections will not be

Photo 2.

Photo 3.



Photos 1 thru 5: Some examples of high resolution color graphics photographed by the author from various high resolution color graphic displays, using techniques similar to those described in this article. Photo 1 is a false color image of farmland obtained from an aircraft by a NASA 24 channel multispectral digitizing scanner. The data was converted and displayed on a high resolution color monitor at the NASA Goddard Institute for Space Studies in New York. Photos 2 and 3 were recorded by LANDSAT satellite and processed by the General Electric Image 100 image analysis system. The LANDSAT system records four black and white images taken in different parts of the light spectrum. After analysis, the Image 100 displays grey scale values or other computer derived features as arbitrary false colors. Photo 4 was recorded from an aircraft and processed on the Image 100 system. Photo 5 is a false color image created at the University of Kansas Center for Research, Remote Sensing Laboratory, using their Identification, Discrimination, Enhancement Combination System (IDECS).



Photo 4.

noticed unless you are consciously looking for them, but they will be obvious in the resulting photographs. If you find that you are unable to eliminate reflections of the camera and yourself, you can overcome this with a simple device. To eliminate the camera reflection, use a piece of black lightweight cardboard or stiff paper somewhat larger than the camera. Cut a round hole in the center of the paper just large enough for the camera lens to fit through, and attach it to the lens with either tape or a filter adapter ring. You can eliminate reflections of yourself by standing to one side of the camera during the exposure. This is facilitated by the use of a shutter cable release, which also guards against camera movement during the typically long exposure times.

There is one case when you might want to intentionally use room light when photographing a display. If you are photographing a vector display or oscilloscope screen as opposed to a raster scan video display, you can use a dim room light to reduce contrast. A desk or table lamp placed behind the display screen is usually sufficient. If you're going to do this often, it might be worthwhile to make a few tests with different lamp intensities to determine the proper ratio of background to display lighting. When using this technique, be conscious of potential reflection problems.

Next, it is necessary to adjust the video display properly. This is the most important factor in obtaining high quality photographs. The use of excessive contrast and/or brightness when adjusting the display can degrade images. For good quality photographs, the display should appear slightly "flat" with lower contrast than used for normal viewing, and there should be absolutely no sign of blooming or smearing of the high intensity areas. You can achieve this condition through an iterative adjustment of the contrast and brightness controls. First, lower the contrast somewhat from its normal setting. Then, adjust the brightness control until you can just see dim grey over the entire background raster where there is no signal present (ie: no image or characters). If, at this point, the image appears excessively low in contrast, turn the contrast up slightly and readjust the brightness to obtain a barely visible background. Alternatively, if the image appears too contrasty, or if the high intensity areas are smeared, turn the contrast down slightly and readjust the brightness. The secret is to obtain a display with a dark grey background raster and slightly lower contrast than you think is proper.

Since this procedure requires qualitative judgement on your part, it is very important to experiment with a test roll of film using several slightly different settings. Throughout the test be sure to record the video display control positions and camera settings for each exposure. Otherwise, by the time you have the developed film ready to evaluate, you will probably find it impossible to duplicate any of the test conditions.

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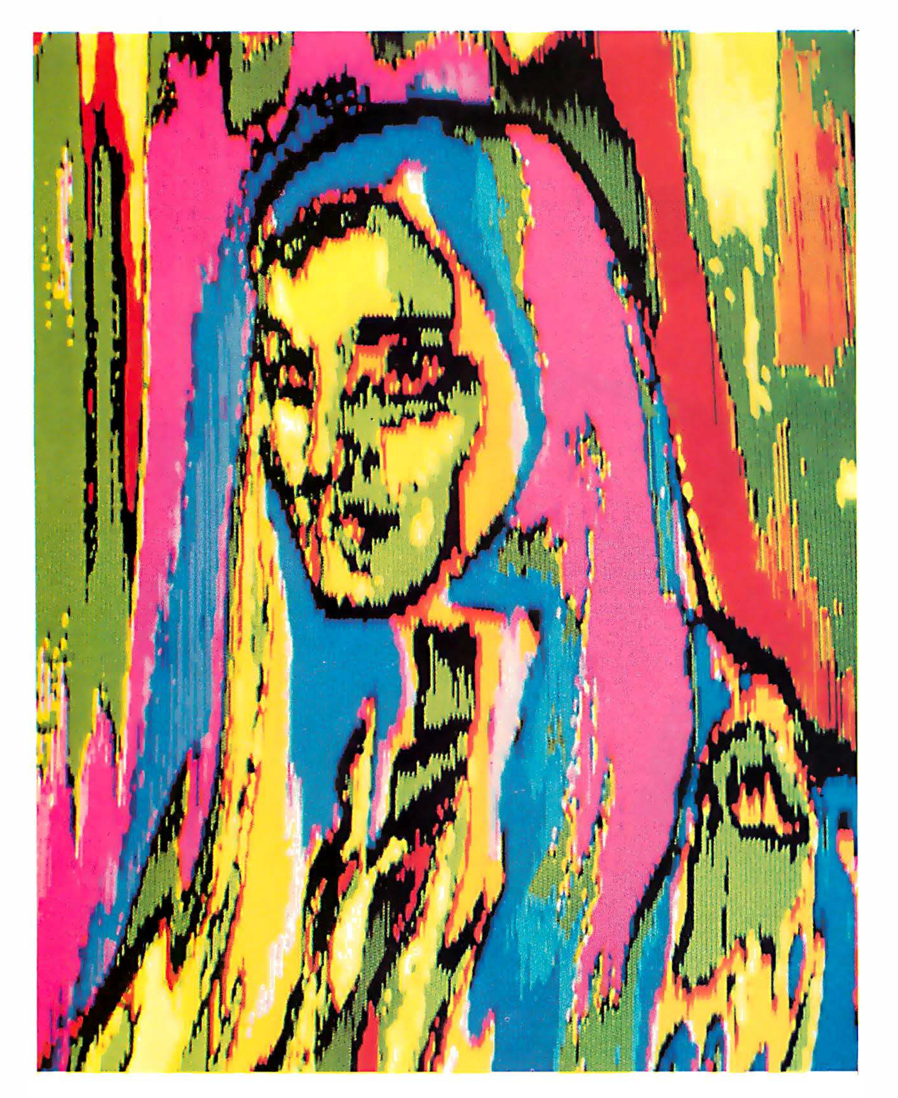


Photo 5.

Although any shutter speed within this range is adequate, I prefer 1/2 or 1/4 second, which usually results in a reasonable f-stop setting with my particular film.

Automatic exposure controls and light meters are only partially effective in this application. In order to utilize these aids, your test display should contain an even mix of light and dark pixels. Or, if you are photographing an alphanumeric display, it should be nearly filled with text. As a rule of thumb, if your display is about 1/2 full of text, decrease the light meter exposure by 1/2 f-stop, and if your display is 1/4 full, decrease the meter exposure by one full f-stop. Also, during the initial tests, it is wise to bracket the determined exposure by making two additional exposures at each test setting: one at one f-stop more exposure, and one at one f-stop less exposure.

The proper film exposure also depends on which film you are using. For color, I prefer Kodak Ektachrome -64 daylight type (ASA 64), and for black and white, Kodak Panatomic-X exposed at ASA 64 instead of the rated ASA 32. With either of these films and a properly adjusted video display, a good starting exposure is 1/2 second at f/4. If you do not have an exposure meter, you can make your initial tests with this basic exposure together with two bracketing exposures of plus and minus one f-stop. If you prefer another film you can adjust the basic exposure according to your film's ASA rating. For example, ASA 125 film requires one f-stop less exposure, and ASA 32 film requires one f-stop more exposure. *[At BYTE we have had good results using the new high speed Kodak Ektachrome (ASA 200), a macro close-up lens with f-stop set using the through-the-lens meter, and 1/15th second exposure in a dark room. The color photos in Carl Helmer's Apple II review, page 18 of the March 1978 issue, were made this way. . .CM]*

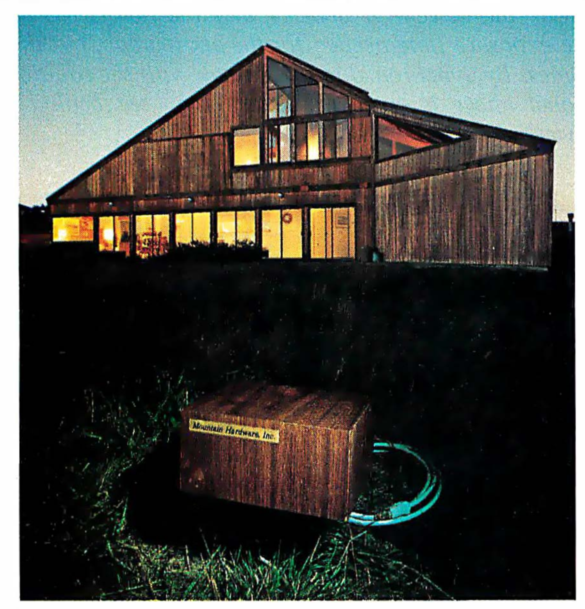
When using color film always use daylight type, not tungsten or indoor type. Daylight film faithfully reproduces the color balance of the video display. Also, I recommend that you avoid color negative films in favor of color slide or transparency film, unless you do your own color printing or are willing to pay the cost of custom color printing.

With a little bit of care, and using these techniques, you should be able to use your camera as a high quality black and white or color hard copy device. But remember: to avoid frustration and to ensure consistently high quality results, it is important to establish, by test, a set of standard settings for both the video display controls and camera exposure.■

input, you can use the results of this test to determine the optimum contrast and brightness settings for your equipment. You can mark these and use them for all photographing. Also, you can achieve the most consistent results this way. However, if you are using capacitor coupled video or RF (radio frequency) input, the contrast and brightness are somewhat data-dependent and you may need to make slight adjustments for different displays. Even in this case, though, a single setting of the contrast and brightness controls can be used most of the time, and marked settings should certainly be used as a constant reference.

When making the initial tests it is also necessary to determine the proper film exposure. For static video display patterns, the shutter speed you use is not critical. The only consideration is that it must be longer than 1/30 of a second, since this is the time required for one complete screen refresh. Likewise, the exposure time should not normally exceed 1 second to prevent problems with film reciprocity failure.

The Ultimate Turn-on



On/off control everywhere-by computer over the AC wiring

Now it's simple and economical to control AC devices remotely from an S-100 or Apple II computer. Mountain Hardware's new Introl™ system delivers on/off commands over the existing AC lines — so you don't have to string a foot of wire!

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Here's how it works. You plug in a single AC Controller board at the computer bus and connect the AC Interface Adapter to any convenient 115 VAC outlet. The AC Controller is now connected to address as many as 64 channels remotely. But it's completely isolated from the 115v power, so there's no chance of short or shock.

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The Calendar/Clock Board for S-100's costs $179 in kit form, $219 assembled and tested.

All prices are f.o.b. Ben Lomond, CA. Prices are USA Domestic. California residents add 6% sales tax.

Where to find it. The Introl system can now be found at computer shops throughout the U.S. and Canada. Drop by and ask for a demonstration. Mountain Hardware, Inc., may be reached at Box 1133, Ben Lomond, CA 95005. Phone (408) 336-2495.

AC Controller (Apple)

Dual Channel AC Remote

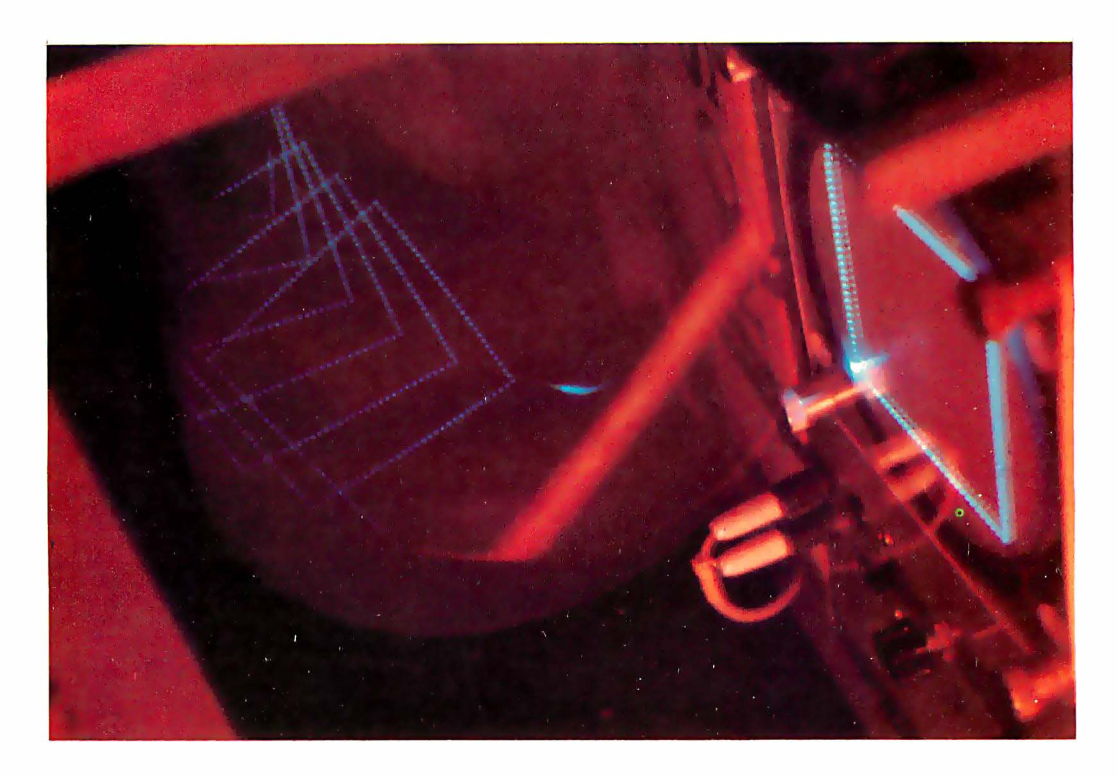
AC Controller (S-100)



Mountain Hardware

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Photo 1: A three-dimensional "square spiral" being generated by the authors' microcomputer controlled display system. At right is an oscilloscope screen displaying a series of points around the perimeter of the screen. It appears that the points are being displayed simultaneously because of the exposure time needed for the photograph, but they are actually being displayed at different times. By synchronizing the display with the rotation of the mirror (at left), a true three-dimensional image is created. Viewers can "see behind" the images, and perspective changes with viewing angle.



Graphics in Depth

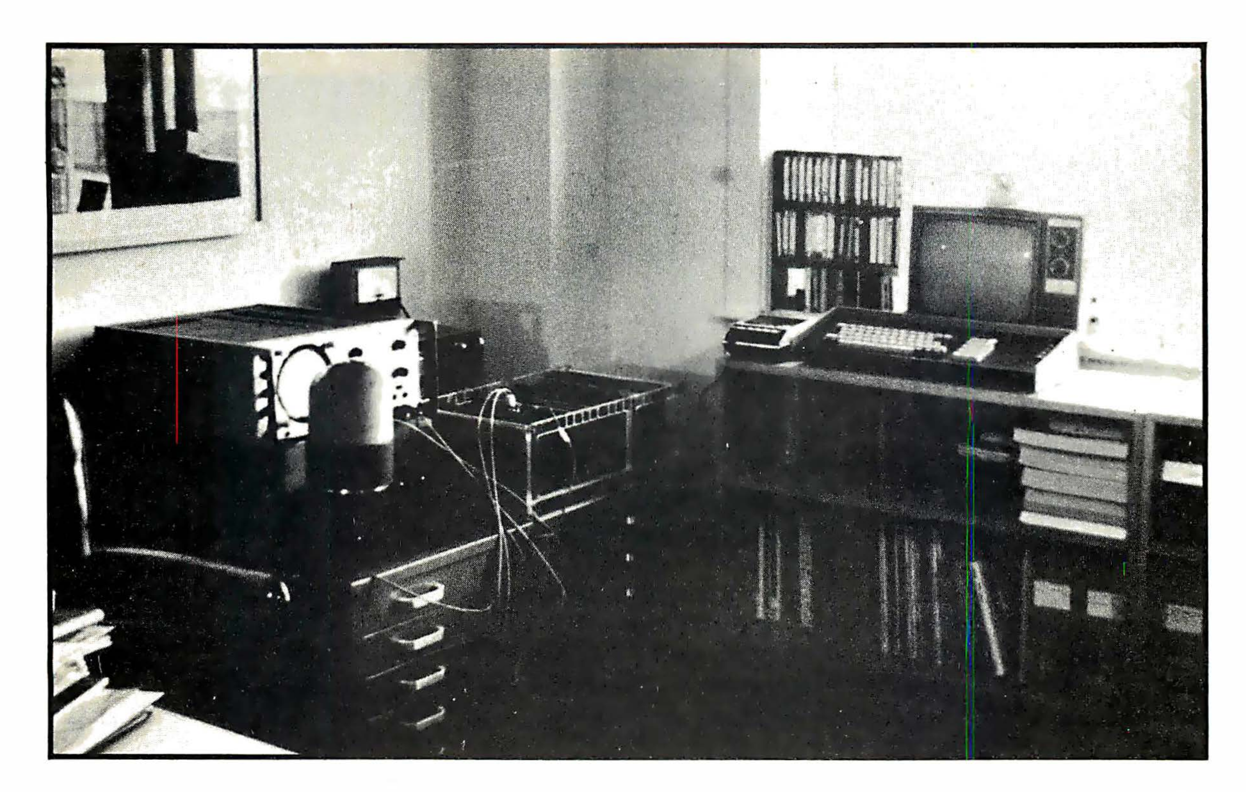
Timothy Walters
William Harris
The Computer Factory
51 Brattle St
Cambridge MA 02138

Introduction

Regular readers of BYTE have already seen many articles and advertisements concerning graphic displays. A graphic display adds direct visual impact to the computer output, communicating directly in a nonverbal manner. The advantages of this kind of display in specific applications are obvious. But what about adding a third dimension to the display?

Many drawings are representations of three-dimensional data in two dimensions; with the ability to display in three dimensions it would not be necessary to use perspective or other cues to suggest an impression of depth. Instead, an architectural drawing, Space War, 3-D Life or abstract graphic designs could be displayed directly. An image displayed in this manner would appear to exist in space; viewers could "look behind" the image to a degree and see it from different perspectives by simply changing their viewing angle.

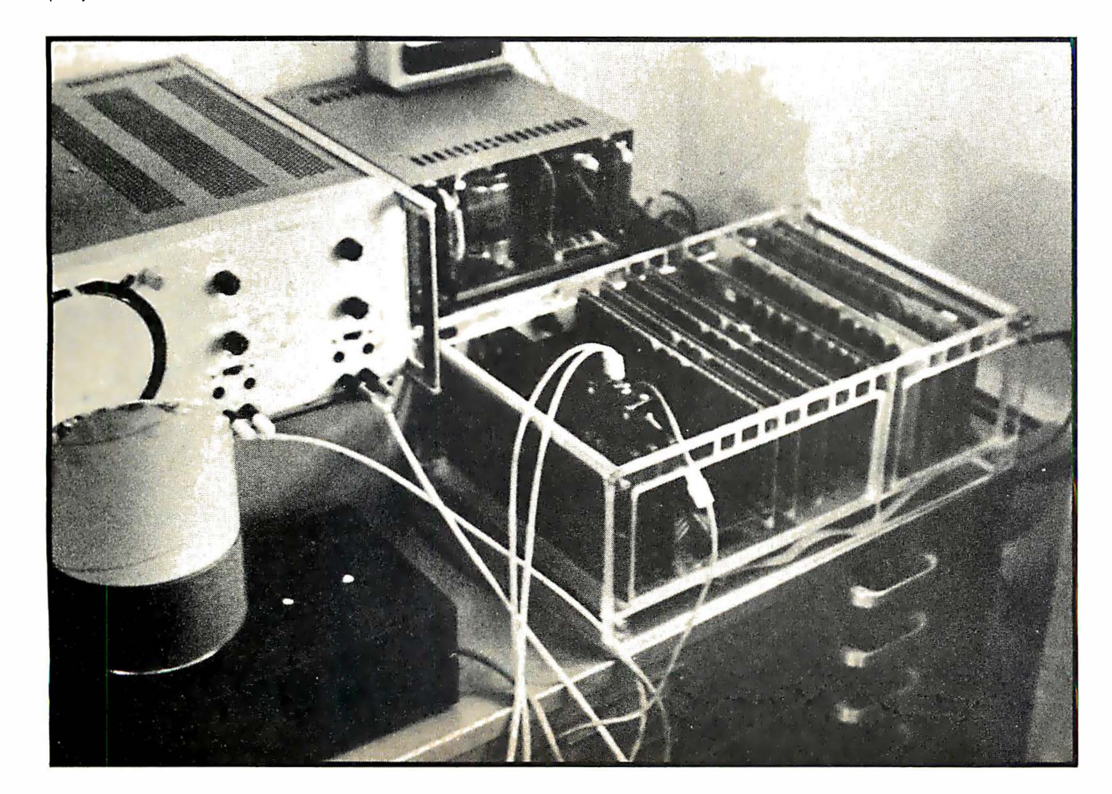
How can a three-dimensional display be built? Several techniques have been used in the past. One general method involves presenting separate views to each eye by means of a special viewing apparatus familiar to anyone who has gone to a 3-D movie or used a stereopticon. Many people find it fairly easy to train themselves to merge two stereo images presented side by side by crossing or "walling" their eyes. This does not require any special viewing equipment, and anyone who is going to view a lot of stereo images might want to learn this technique. Since it does require some training an untrained friend may not be able to view a graphics demonstration in a full three dimensions without the special apparatus.



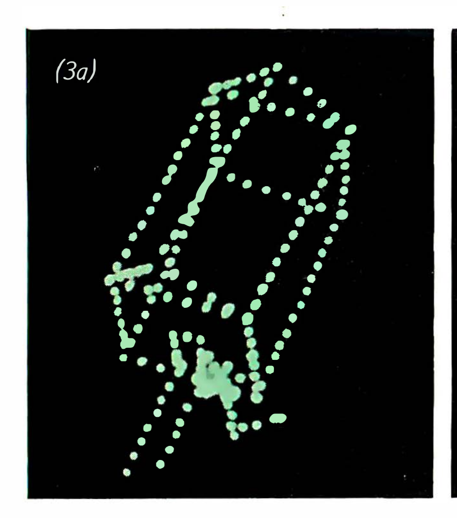
(2a)

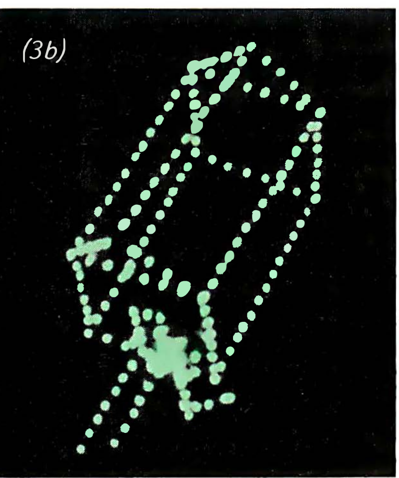
3-D Adds a New Dimension to Your Display

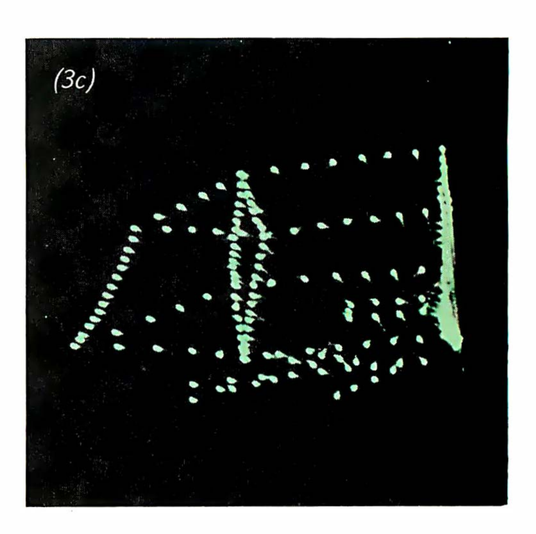
(2b)



Photos 2a and 2b: The authors' laboratory. Photo 2b shows a close-up of the 3-D display apparatus. The mirror is shown at left mounted on its cardboard tube, with the oscilloscope behind it. The Digital Group computer mainframe is at right.







Photos 3a, 3b and 3c: Photos 3a and 3b were taken from slightly different angles to form a stereoscopic pair. The image is generated by the program in listing 3; readers can view the image in 3-D using the techniques described in the text. If you have access to a stereopticon, it may facilitate the process. Photo 3c shows the distorted image of the house as it appears on the oscilloscope screen. It should be emphasized that photos 3a and 3b show the three-dimensional effect of the display at only one *viewing angle; the actual effect of looking down into the rotating mirror is much more realistic because the image changes shape as the observer's viewing angle changes within a cone of visibility.*

An example of separated stereo pairs is shown in photo 3. The images may be merged together by focusing the eyes at a distance until the two blurred images merge, and then focusing the eyes on the images without letting the images separate. One way to aid the eyes to merge these two images is to use two paper tubes to look at the images. With practice, the eyes will be able to view the image comfortably and without strain. With this technique, the right eye views the right image and the left eye views the left image. The differing positions of the various lines in the two images are matched up and interpreted by the brain as if they correspond to real lines at different depths. Viewed properly, the house should appear as it would from an aerial view. If the pairs are merged in the opposite manner (by crossing the eyes to look at a point close to the observer and then refocusing), the apparent angles are reversed and the house will appear to turn "inside out." This technique may be aided by focusing the eyes on a finger held above the page. If you are unable to fuse stereo images by moving the eyes, it may be necessary to purchase a stereo viewer from an optics supplier to view this kind of display.

It is quite easy to generate these stereo images on a high resolution plotter or graphics terminal by calculating the appropriate perspective views for each image. This produces realistic three-dimensional images when viewed properly; however, they are not auto-stereoscopic, that is, they do not appear to be stationary three-dimensional objects when the observer moves around to different positions. Instead, they appear to move around to *follow* the observer. However, with some mechanical construction, a display system can be constructed that produces a true three-dimensional image viewable from a wide range of observer positions. The hardware and software system described in this article can produce displays containing up to 2000 points with a posi-

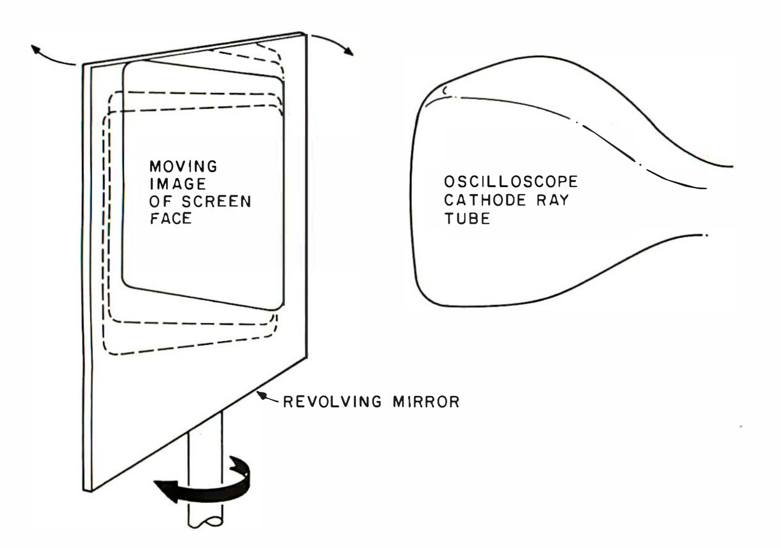


Figure 1: One method for generating a three-dimensional display. A vertical mirror is rotated in front of an oscilloscope screen. A volume of space is thus defined in which points can be made to appear by displaying them on the screen at the right time. One disadvantage of this method is the relatively restricted viewing area caused by the position of the oscilloscope.

Continued on page 116

extensys presents

EX3000—a new multi-user multi-tasking computer system.

This complete series of computer systems embody architectural concepts previously found only in costly large scale computers. The primary concepts used in the EX3000 computer systems are distributed processing for hardware and multi-tasking for system software. The EX3000 systems distribute system processing functions to those system components that are best suited to perform those tasks. This state-of-the-art technology was prohibitive until the recent introduction of cost effective computational and control microprocessors, along with programmable peripheral circuits to perform preassigned dedicated tasks. Coupling these cost effective components with the distributed processing techniques proven by many large mainframe computer manufacturers, Extensys Corporation has been able to provide exceptionally powerful and flexible systems. Through the efficient use of system components in a modular structure, the EX3000 Computer Systems allow configurations that meet a wide variety of specific applications as well as offering expansion capability to satisfy increasing usage demands.

The hardware of the EX3000 Computer Systems consist of subsystems and boards. Three subsystems are provided:

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Other p/c boards which are included in the EX3000 system are:

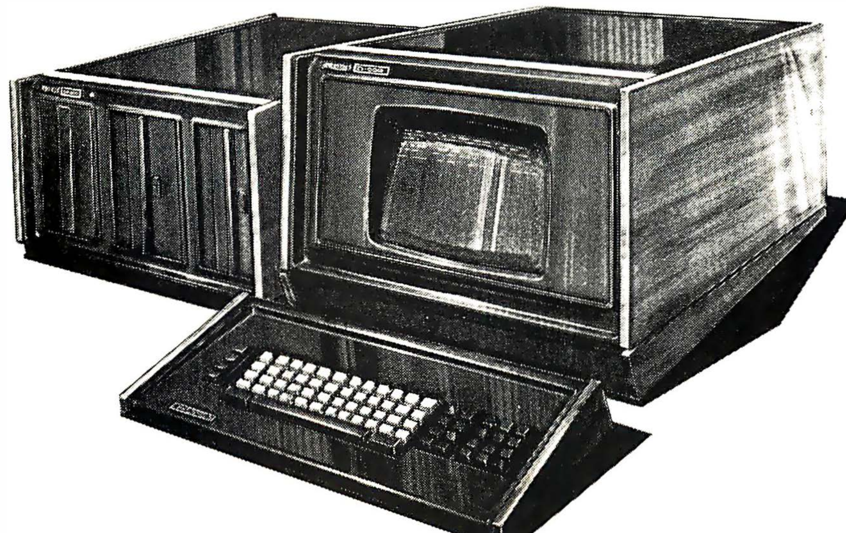
- RM650 Memory board with 16K to 64K bytes of RAM storage.
- MM16 Memory Management board with bank switching up to 1 megabyte of RAM memory and a priority DMA mechanism for high speed DMA transfers.
- MPU805 8085 Central Processor with on-board PROM space (16K), prioritorized vectored interrupts, and combination interval timers/event counters.

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* Apple II plugs into any standard TV using an inexpensive modulator (not included).

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Convert Your TV Set to a Video Monitor

Dan Fylstra
22 Weitz St #3
Boston MA 02134

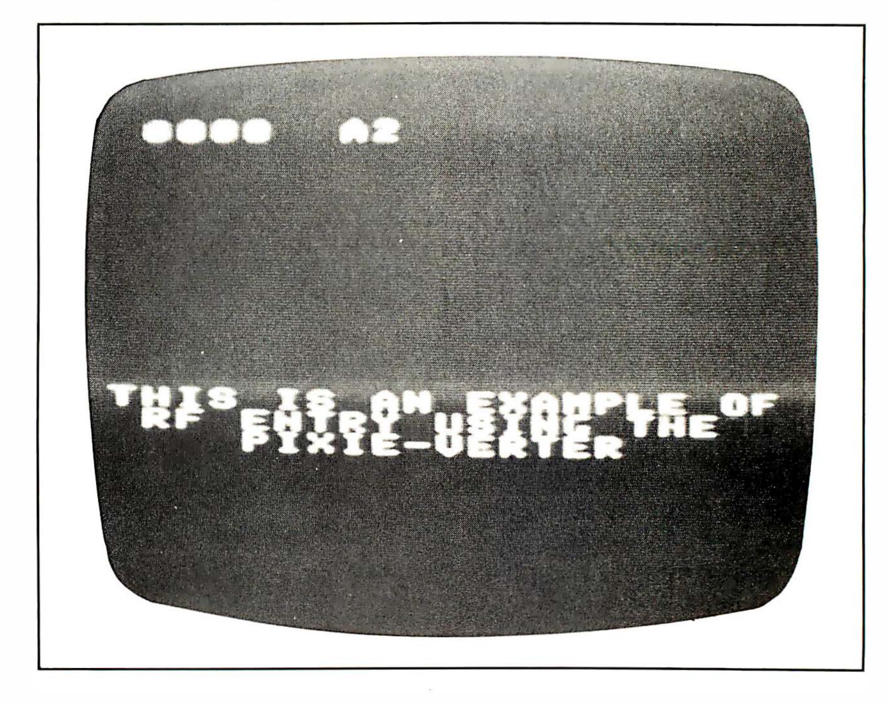


Photo 1: This display, produced by an ATV Research Pixe-Verter driven by an Ohio Scientific Instruments Model 440B video board, illustrates the RF modulator method of adapting an ordinary TV set to serve as a video monitor. This method requires no modifications to the TV set, but limits the number of characters that can be displayed on one line.

Most modern personal computers are designed to display lines of characters and possibly graphics patterns on a video monitor. This is an ideal way to provide high speed readable output of alphabetic and numeric information at a low cost. Unfortunately, video monitors themselves are still rather expensive. Examples are the 9 inch (27.4 cm) Javelin monitor at $175 and the 9 inch Hitachi monitor at $185. A few surplus video monitors are sold for prices (which I have seen) ranging from $90 to $150, but these may be hard to find, difficult to interface, lacking cabinets and possibly unwarrantied. All standard monitors can be used only for dedicated display applications and will not receive regular television programs.

Many computer experimenters have adapted regular television sets for use as video monitors. This may be done either by building an "RF modulator," in effect a tiny TV transmitter that clips onto the antenna terminals of the TV set feeding the computer generated video signal in like any other program, or by physically modifying the TV set, cutting off the video signal coming from the airwaves through the video detector, and feeding the computer's video signal into the set's video amplifier. (With some care, a switch can be added to permit either normal program reception or computer generated display.) The principles behind these two methods and sample circuits have been seen in the pages of BYTE from time to time. (A complete guide to video signal generation, TV set modification and related topics will be found in Don Lancaster's book, *TV Typewriter Cookbook,* Howard W Sams and Company, Indianapolis, 1976.)

This article is a personal use review of two of the most popular kits for TV

Continued on page 131

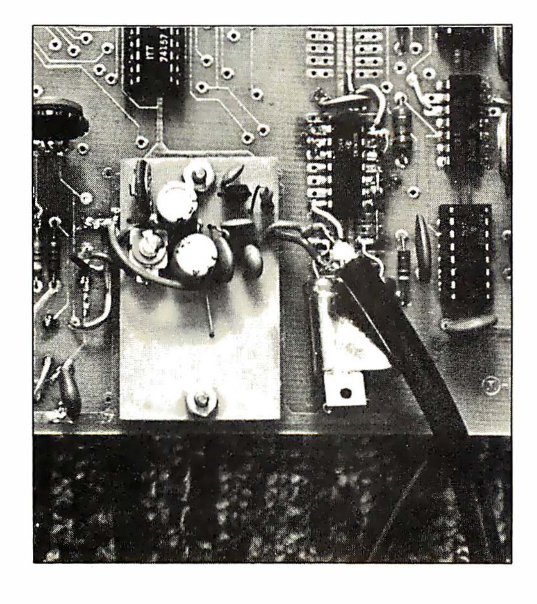


Photo 2: The Pixe-Verter mounted in the space provided on the OSI 440B video board. The other end of the shielded cable is attached to the antenna terminals of the TV set. The assembly should be mounted inside a metal box to prevent interference on other TV sets in the vicinity.

Product Description:

The Matrox ALT-256 Video Board

Gary Ruple
Matrox Electronics Systems
POB 56 Ahuntsic Sta
Montreal Quebec H3L 3N5
CANADA

The ALT-256 is an Altair (S-100) bus compatible graphics card that gives a resolution of 256 by 256 dots. This display is useful for professional graphics applications such as computer aided design, simulation, business and educational displays, and plotting curves.

The display memory on the ALT-256 consists of 16 4 K dynamic memory integrated circuits in the 16 pin package. The dynamic memory refresh is handled by the video scan circuitry so that no processor time is required for this function.

Board Addressing

The board is addressed as four contiguous output ports and one input port (IO ports are built in), selectable by on board address jumpers. The dot addressing is done in X–Y fashion. Output ports 1 and 2 are used as registers for the X and Y positions, respectively, to position the cursor at the selected dot. Output 0 is used to write the intensity of the dot: 00 for black and 01 for white. After the dot intensity is loaded, the ALT-256 will require 3.4 μs to write the dot in the display memory (ie: to allow for internal synchronization of the wire operation, video read scan and dynamic memory refresh). Since the 8080 processor almost always requires more than 3.4 μs to load the next dot address and data, the processor can run at its full speed. Also, there will be no streaks or flashes on the display no matter how fast the

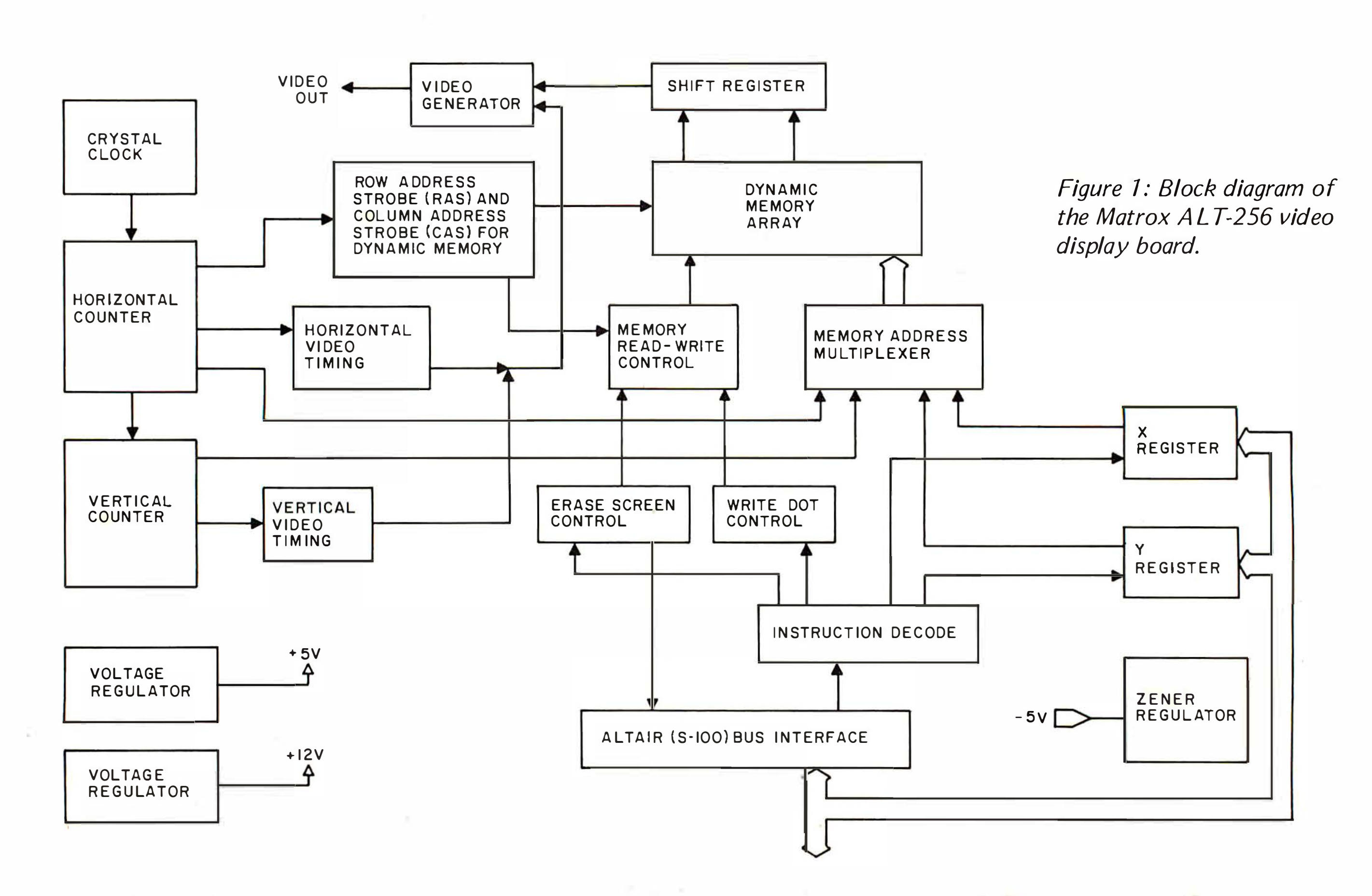
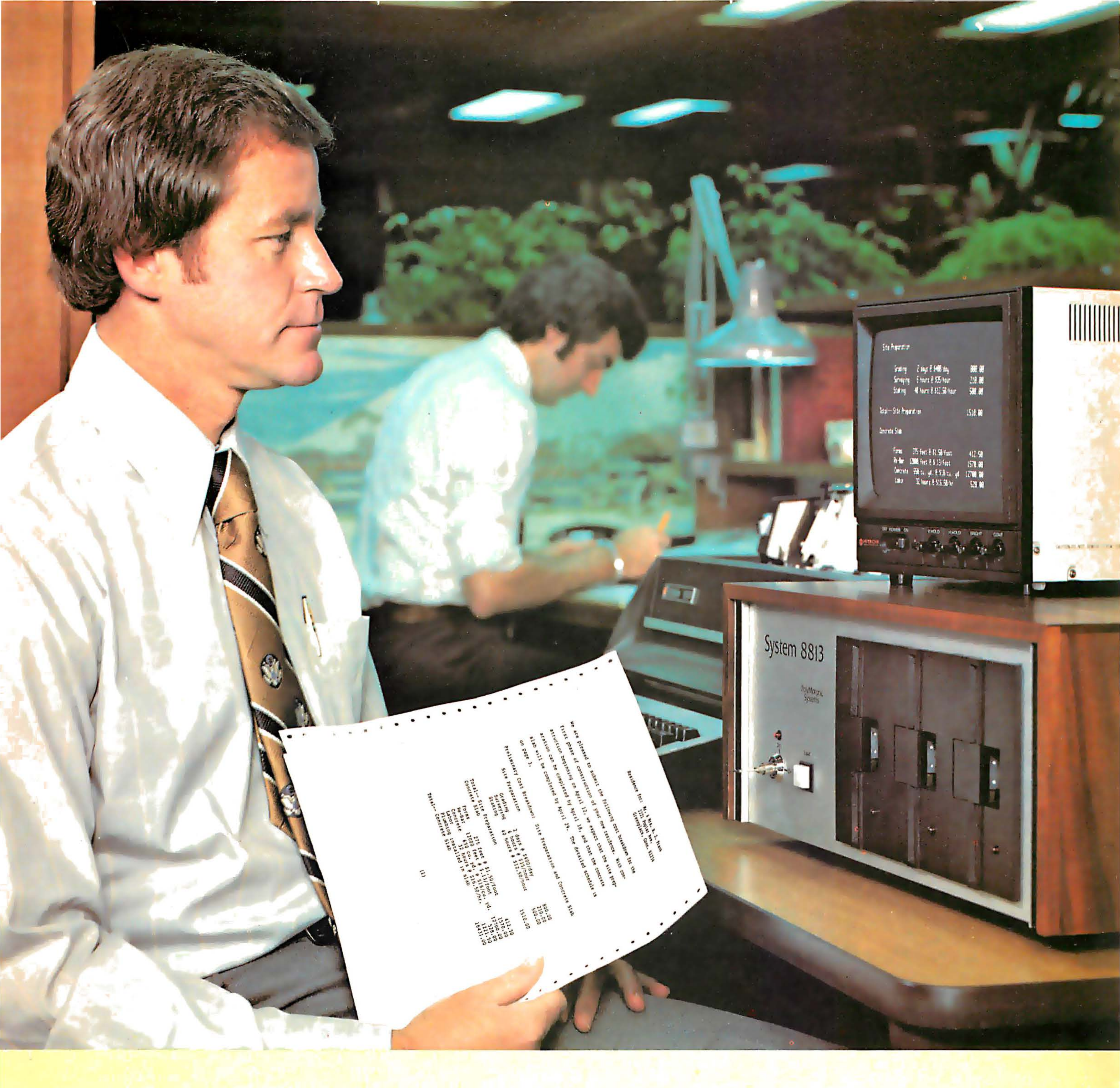


Figure 1: Block diagram of the Matrox ALT-256 video display board.


System 8813
PolyMorphic Systems

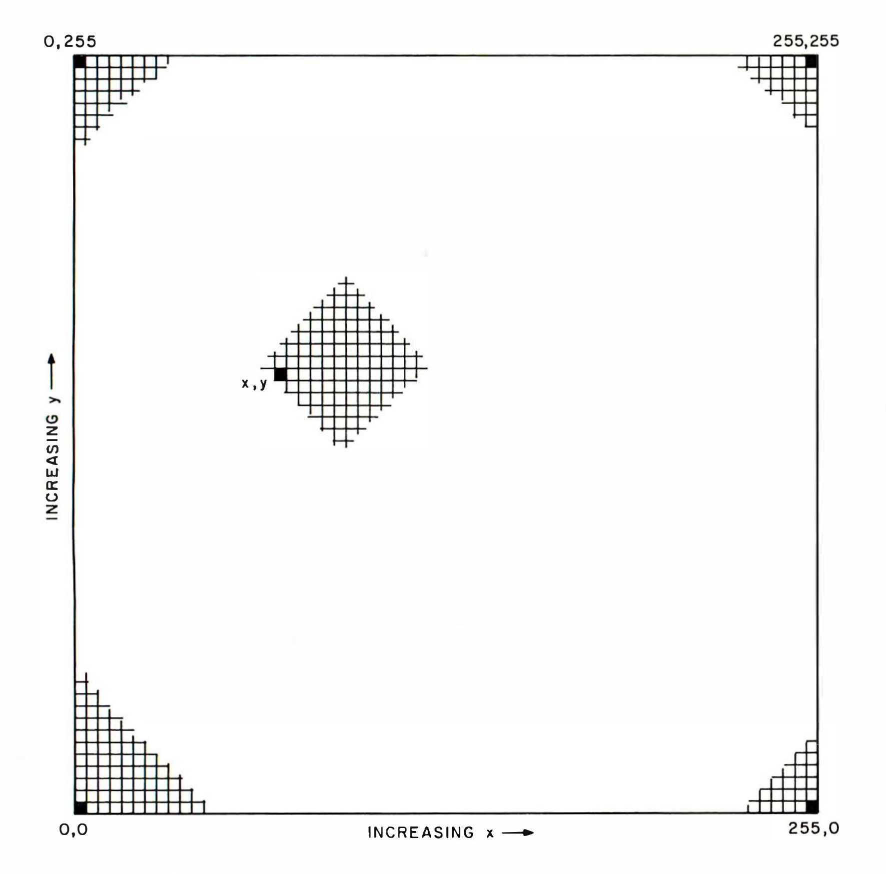


Figure 2: Display coordinate system for video displays (MTX-Graph software).

processor accesses the card since the write operation is internally synchronized.

Output port 3 is used as an erase screen command to either clear the screen or to set it all white according to data bit 0: 0 = black, 1 = white. The erase operation can take up to 33 ms. The status port (IN0) has been provided as a means of checking the status of the ALT-256. The following is a description of the status bits:

Bit 0: When 0 the display is ready. When 1 the display is being erased and should not be accessed.

Bit 1: When 0 the display scan is in the video portion. When 1 the display scan is in the vertical blanking period allowing access of the display when not visible. This is useful for dynamic motion and animation synchronization.

The X–Y addressing scheme provides the programmer with a way to address individual dots. A horizontal or vertical line requires only one address to be updated for each new dot. A 45° diagonal requires each address to be incremented or decremented. Using output ports as registers and as a means of addressing the card also conserves memory space, since the 65,536 directly addressable dots are equivalent to 8 K bytes of memory. (You would also have to keep track of dot position in the byte.)

Theory of Operation

The ALT-256 has four major blocks: the video sync generator, scanning circuitry, cursor and interface electronics, and 65,536 by 1 memory (see figures 1 and 2). The sync generator consists of a crystal oscillator and a divider chain. This divider chain produces all timing signals for the memory scanning as well as horizontal and vertical sync. The video sync generator can be programmed by jumpers for either the European or the American video standard.

The scanning circuitry consists of multiplexers which provide proper address, and read and write signals for the programmable memory.

The cursor consists of two 8 bit latches (the X and Y address registers) which are loaded by the processor. Necessary interface address and timing decoding is accomplished by the Altair (S-100) bus interface logic.

The refresh memory has 16 4 K dynamic memories (IC type 4096) organized as a 65,536 by 1 bit memory.

Power supplies for 5 V, 600 mA; 12 V, 100 mA, and −5 V, 10 mA are generated by on board voltage regulators.

Multiple Boards

The ALT-256 may be used in multiple board systems for color graphics or grey scale applications. Any reasonable number of boards may be used. When more than one is used, one board must be chosen as the master and the others are configured as slaves synchronized to the master. There is an on board jumper allowing use as a master or slave and a socket provided for connecting the sync signals and video between master and slaves. Single or multiple boards may also be slaved to an external sync generator such as a TV camera signal or broadcast video.

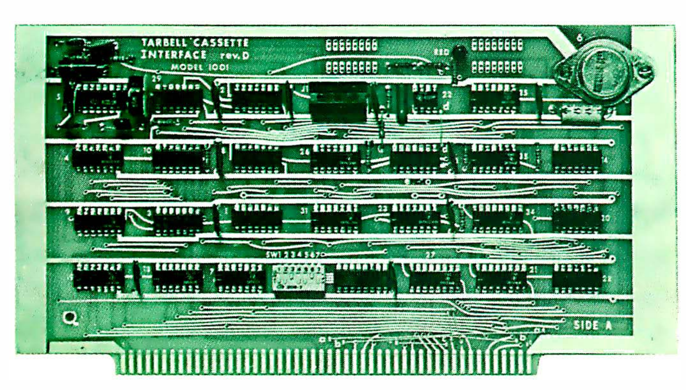
Software

MTX Graph, the software package available for the ALT-256, provides all the commonly used low level graphics routines, and is configured as a series of subroutines that occupy hexadecimal memory locations 0104 to 04FF. Multiple boards can be supported by up to a maximum of eight bits of color or grey scale information. Features of the package are described in table 1.

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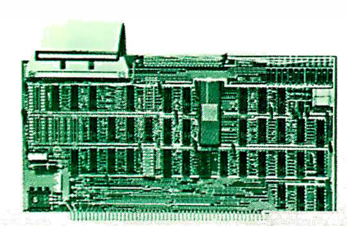


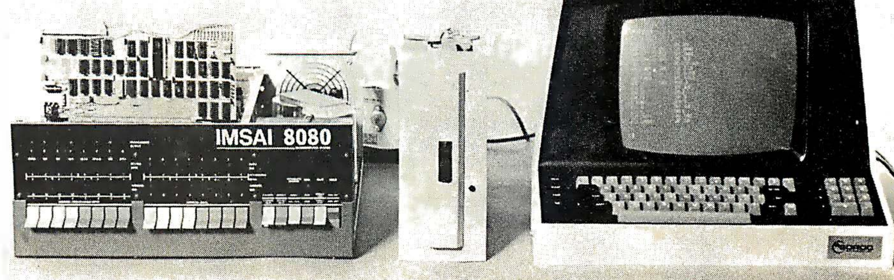
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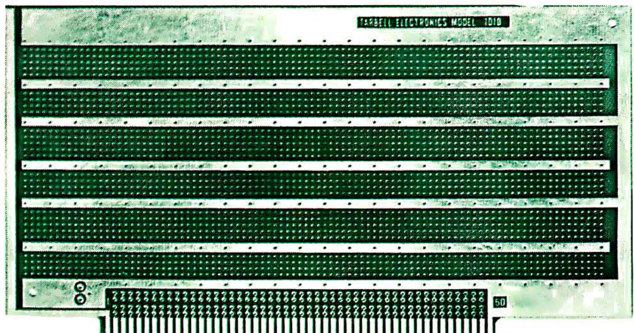
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Circle 360 on inquiry card.

Photo 1a.



Photo 1b.



Photo 2a.

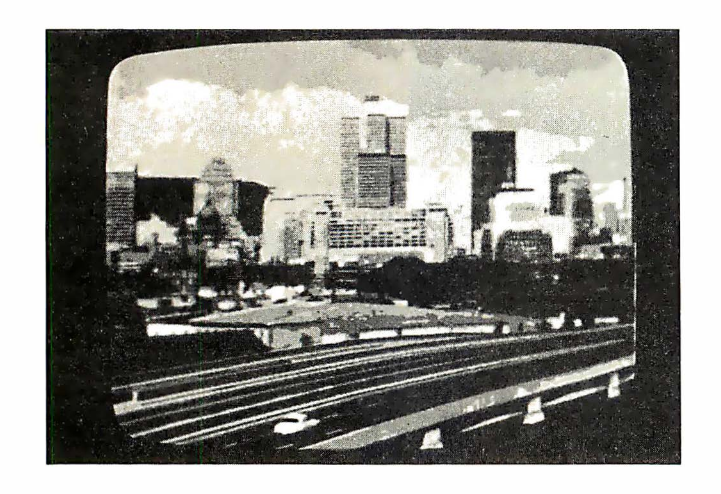


Photo 2b.



Photo 3a.



Photo 3b.



Photos 1 to 3: Some examples of grey scale and pseudocolor images produced by the ALT-256 video board. The grey scale photos were produced by feeding the output from a TV camera through a slow scan analog to digital converter. Next, the 3 bit digitized output was processed through three ALT-256 video boards and a digital to analog converter to give an 8 level video signal. The color pictures were produced by feeding the outputs from the video boards directly to the red, blue and green inputs of an RBG color monitor (see figure 3).



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Circle 285 on inquiry card.

Table 1: Features of MTX GRAPH, a software package available for the ALT-256 graphics board.

1. **Variable Resolution:** The display resolution may be set to 256 by 256, 128 by 128, or 64 by 64 through software control.
2. **Point Plot:** A dot corresponding in size to the resolution selected may be displayed at any arbitrary point by specifying X-Y coordinates.
3. **Line Vector Graphics:** Lines can be drawn from the current cursor position to the endpoint specified by the user.
4. **Alphanumeric Display:** A full ASCII character generation routine is provided. Characters can be positioned anywhere on the screen. Carriage control characters are correctly interpreted. Character size is adjustable.
5. **Animation Synchronization:** This feature is used to synchronize animated display updates with the vertical scan.
6. **Color Option:** The software package supports a 3 card color or grey scale system as described later in this article.

All subroutines use standard Cartesian coordinates with the display occupying the first quadrant. As shown in figure 2, the origin (X = 0, Y = 0) is defined as the bottom left point on the display. X increases in value to a maximum of 255 at the right edge, while Y rises to a maximum of 255 at the top. If the ALT-256 is jumpered for American Standard scan (240 lines displayed), the lowest Y coordinate displayed is 16, and points with coordinates from 0 to 15 cannot be seen.

Grey Scale and Color Applications

In the grey scale configuration, multiple boards provide binary intensity information. All boards have the same address decoding and sync signals. Each board has a dot intensity bit (output port 0) which is normally tied to data bus bit D0. In a typical 3 board color or grey scale system, the intensity bit is changed on two boards to be D1 and D2 (or any other bits you choose), thus writing three binary bits for each write operation. This method allows computation of grey scale and single instruction load of all bits making up a single picture element (often contracted to "pixel" in graphics literature). The TTL video outputs from the three boards are fed to a simple 3 bit digital to analog converter.

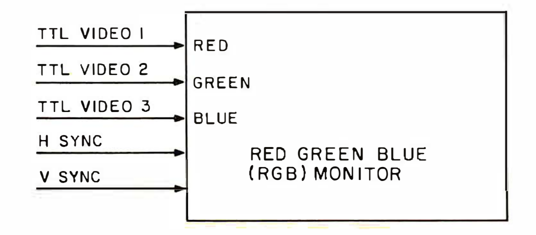


Figure 3: Connecting an RBG (red green blue) monitor for 8 color operation using three ALT-256 boards.

RGB (Red Green Blue) Color

In a color scheme, the best results are obtained by directly driving the red, green and blue guns of a color monitor with the video signal from three boards, as in figure 3. An ordinary color TV can be modified to accept separate color inputs. This should not be undertaken by anyone who lacks an understanding of color TV and electronic design. The alternative is to generate an encoded composite color signal. An application note available from Matrox gives details on a color encoder circuit.

Photographs

The photos accompanying this article were generated by feeding a TV camera output through a slow scan analog to digital converter. The 3 bit digitized output was then fed to a 3 card ALT-256 graphics system. The grey scale pictures were produced by feeding the outputs of the three cards to a 3 bit digital to analog converter. The resulting pictures have eight discrete grey levels. The color pictures were produced by feeding the outputs of the three cards to the red, blue and green (RBG) inputs of an RBG color monitor. The resulting eight color pictures are pseudocolored. This means that a different color has been assigned arbitrarily to each grey level in the original picture. Pseudocoloring is used in many industrial and research applications (ie: many NASA space pictures are processed this way).

Conclusion

The Matrox ALT-256 represents one approach to high resolution graphics capabilities for the Altair (S-100) bus. Multiple board systems can be used for medical displays, research applications, pseudocolor imaging, fast animated displays, computer aided design, sophisticated computer games and computer generated art. For the Star Trek freak, now there is available a real (if imaginary) universe to save, rather than a slow printer banging out descriptions. For the artist, a canvas; the researcher, a window; and the kids, an electronic sketch pad.■

Note: The completely assembled, tested and burned in ALT-256 board is available for $395 from Matrox Electronic Systems, POB 56, Ahuntsic Station, Montreal, Quebec H3L 3N5 CANADA. Also available is the ALT-2480, an Altair (S-100) compatible alphanumeric generator board, which can be used in conjunction with the ALT-256 to produce simultaneous graphics and alphanumeric displays.

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Color Graphics on the Compucolor 8051

The ancient wisdom that says "a picture is worth a thousand words" has a special significance for the computer age. With machines that can generate output faster than anyone can read it, there's no doubt that we need new ways to represent this avalanche of data. The best answer (so far) seems to be in computer graphics: sophisticated pictures that show the results of all this computation in a form that is easy to interpret and even easier to remember.

One of the most dramatic ways to improve graphical output is to add color. Color graphics conveys information to human viewers that is hard to appreciate until it's experienced. The change from black and white to color is at least as impressive as the change from monaural to full stereo sound.

Until a few years ago, the hardware for color graphics was both rare and expensive. This situation is changing, however, mainly through the efforts of manufacturers who have devised ingenious ways to use the technology of color TV in conjunction with computer technology.

One of the first products designed for this purpose was the Cromemco TV Dazzler. It consists of two Altair (S-100) compatible boards with a coaxial cable output to a color monitor. Several examples of color art produced with the TV Dazzler were shown in December 1976 BYTE. That issue also contained the article, "The Cybernetic Crayon," that gave an example of an 8080 assembly language program for the Dazzler.

Photo 1: The Compucolor 8051 with extended ASCII keyboard and "floppy tape" storage. The tapes are similar to 8 track music cartridge tapes, except that they are shorter. More recent models use a floppy disk system for storage.

The Compucolor 8051

A more recent example of personal color systems is the Compucolor 8051. It comes in the form of a complete computer system packaged in a cabinet not much bigger than a 19 inch color television. That's impressive because the cabinet contains the processor, memory, interface, programmable read only memory, graphics controller, power supplies, and a 19 inch color display tube. The colors are of much greater purity than those usually seen on TV because the system uses a very wide bandwidth (75 MHz) and the three color circuits (red, green, blue) are kept separate. This is the same approach used in professional color monitors. Since any of these colors can be on or off, eight colors (including black) are available.

Photo 1 shows a typical system consisting of the computer and color display in the large cabinet, a keyboard for input, and a dual 8 track tape cartridge unit for mass storage.

The large screen holds 48 lines of 80 characters each, about four times the number of lines found on most video displays. When characters are used for graphics, there are 3840 plotting positions available. But a finer division of each character into a 4 by 2 array of "points" is also possible, as figure 1 indicates. In point plot mode, one character

block becomes eight "point" positions. Each of these points (which is really a small rectangle) can be turned on or off separately. This means there are 160 point positions for the horizontal direction (X axis), and 192 points for the vertical direction (Y axis). So a total of 30,720 points can be plotted.

A special hardware feature called "vector graphics" is also available. This makes it possible for the computer to draw approximations to straight lines on the screen if you simply tell it where to start (X0, Y0), and where to finish (X1, Y1). The hardware calculates all the point positions in between and plots them automatically.

The Compucolor 8051 comes with a BASIC interpreter stored in read only memory. This means that you never have to load BASIC: you call for it by just pressing two keys (Escape, followed by W).

The BASIC interpreter has all the standard features and a few extra ones (including string arrays). It also has the special key word PLOT. This feature makes it easy to program graphics of all kinds in color. Let's look at some examples of how it works.

Using Compucolor BASIC

The word PLOT is used in BASIC statements of the form

```
25 PLOT I
```

where I is an integer from 0 to 255. When PLOT I is initially used, the value of I determines what *mode* you enter. There are quite a few modes. The main mode is "point plot" (PLOT 2). After you enter a "mode," the meaning of PLOT I is different, and it depends on what mode you're in.

Example 1: Suppose we want to plot the curve $Y=X^2$. We first use PLOT 2 to put the program in point plot mode. After saying PLOT 2, each pair of PLOT statements that follow will then give the X and Y positions of the point to be plotted. When finished plotting points, we use PLOT 255 to escape from the plot mode we're in. Here's a program that plots 100 points of our curve:

```
10 PLOT 2
20 FOR X = 0 TO 99
30 LET Y = INT(X*X/100)
40 PLOT X:PLOT Y
50 NEXT X
60 PLOT 255
```

To understand the output of this program you have to know that the "origin" for point plot mode is the point (0, 0), and that it is located in the lower left corner of the screen. All points (X, Y) must be described

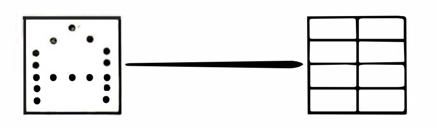


Figure 1: Division of screen character into a 2 by 4 array of "points."

by positive integers with X going from 0 to 159, and Y going from 0 to 191. To make Y=X*X fit on the screen, we divided by 100 (because when X=99, Y=9801 which would be way off the screen). Our graph will look something like the one in figure 2.

Example 2: Here is a program to plot a sine function. We let X go from 0 to 159, but actually plot SIN(X/13). This causes the argument of SIN to go from 0 to slightly over 12 radians, giving about two cycles of the function. Since the SIN function has values from −1 to 1, we multiply it by 95 and then add 95. This causes Y to go from 0 to 190. The program is initiated by the command PLOT 12, which means "clear screen."

```
10 PLOT 12:PLOT 2          'Clear screen, enter plot mode
20 FOR X=0 TO 159          'Get X
30 Y=95*SIN(X/13)+95       'Calculate Y
40 PLOT X: PLOT Y          'Plot X, Y
50 NEXT X                  'Back to line 20
60 PLOT 255                'Exit plot mode
```

Adding Color

The preceding programs plot in whatever color the machine was using last. Color can be changed with either the PLOT 6 or the PLOT 29 modes. After entering the PLOT 6 mode, the statement PLOT I produces various combinations of foreground colors, background colors, and "blink" states, all depending on the value of I. For example, I = 0 to 7 gives the eight possible foreground colors on a background of black with no blink.

The PLOT 29 mode is a little simpler. It allows only foreground (which means the actual point being plotted) color to be specified. It is followed by PLOT I, where I specifies color according to the codes: 16=black, 17=red, 18=green, 19=yellow,

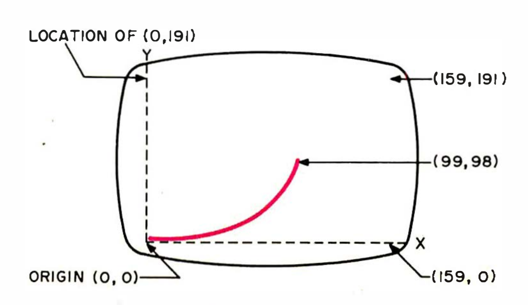


Figure 2: A display of the equation $Y=X^2$.

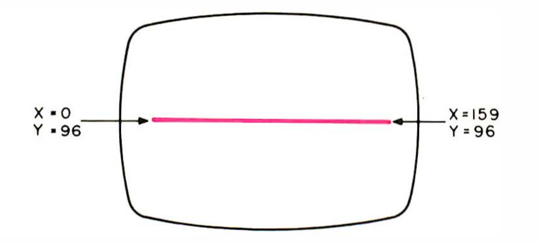


Figure 3: A display of the line running from points (0,96) to (159,96).

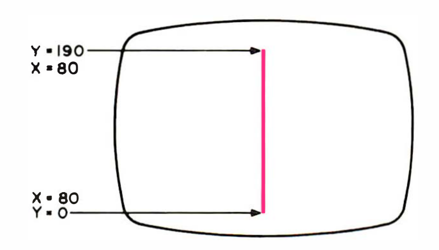


Figure 4: A display of the line running from points (80,0) to 80,190).

```
10   PLOT 12                                     'Erase screen
20   PLOT 29: PLOT 19                            'Set color= yellow
30   PLOT 2                                      'Go into main plot mode
40   PLOT 246: PLOT 0: PLOT 0: PLOT 190          'Plot Y bar graph
50   PLOT 250: PLOT 0: PLOT 95: PLOT 159         'Plot X bar graph
60   PLOT 255                                    'Exit plot mode
70   FOR X = 0 to 159                            'Get X
80   PLOT 29: PLOT 17+X/22                       'Set a color depending on X
90   Y = 95*SIN(X/13)+95                         'Calculate Y
100  PLOT 2                                      'Point plot mode
110  PLOT X: PLOT Y                              'Plot one point
120  PLOT 255                                    'Exit plot mode
130  NEXT X                                      'Back to line 70
```

Listing 1: A BASIC program for graphing a sine function in seven different colors.

20=blue, 21=violet, 22=cyan (light blue), and 23=white.

We'll illustrate this feature in a moment, but let us first look at an example of a subplot mode (a mode that follows the PLOT 2 main mode).

Bar Graph Mode

After entering PLOT 2 mode, you can go into several subplot modes. For example, PLOT 250 means enter the X (horizontal) bar graph mode. It is followed by three PLOT statements that tell where to put the bar graph and how long to make it.

```
PLOT 2: PLOT 250
PLOT 0: PLOT 96: PLOT 159
```

This directs the program to draw a horizontal bar (line) from X=0 to X=159, 96 units up on the screen (the Y position). See figure 3. The code for Y (vertical) bar graphs is PLOT 246.

```
PLOT 2: PLOT 246
PLOT 0: PLOT 80: PLOT 190
```

The latter draws a vertical bar (line) from Y=0 to Y=190, 80 units to the right (the X position). See figure 4.

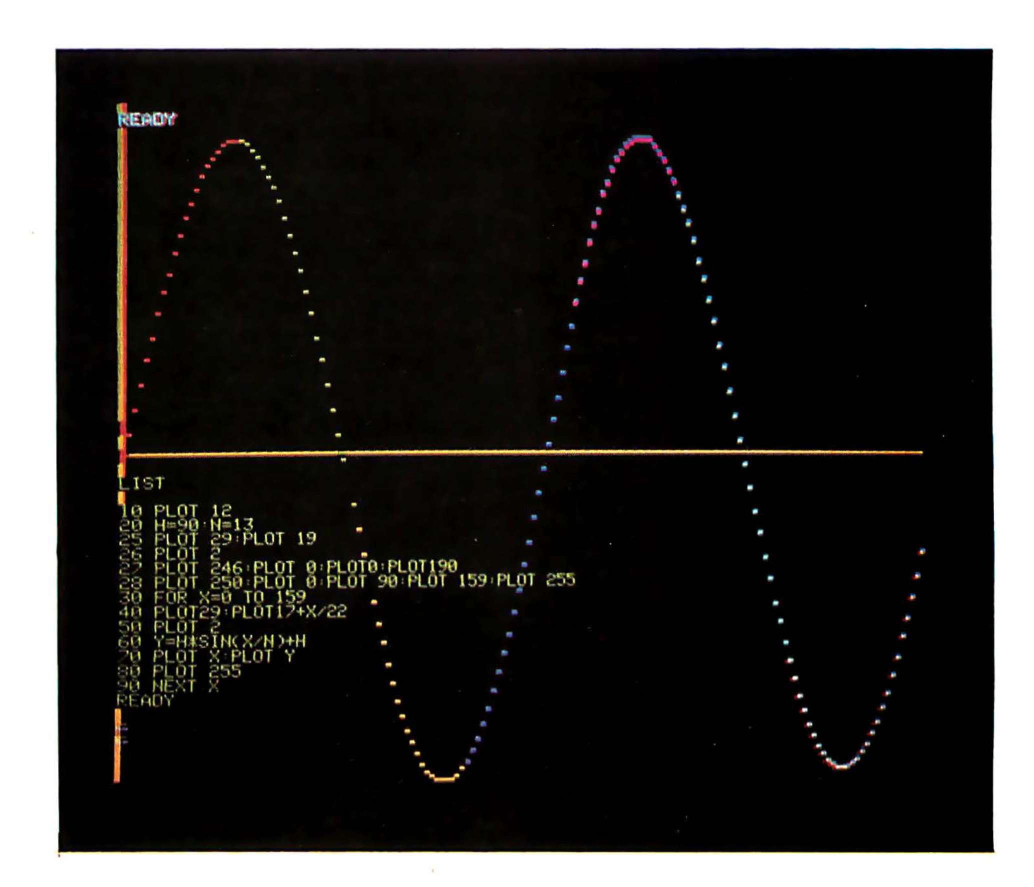


Photo 2: A plot of the sine function, which changes the color of the plotting point cyclically. The axes are drawn with bar graph mode.

A Combined Program

The program shown in listing 1 graphs the sine function using seven different colors (codes 17 to 23). It also uses the bar graph mode to plot the X and Y axes for the graph. The axes are drawn in yellow (code 19). The output of this program is shown in photo 2. Notice in line 100 that PLOT 2 serves a dual purpose. It puts the machine in both main and point plot mode. A more interesting example of the output possible from bar graph mode is shown in photo 3.

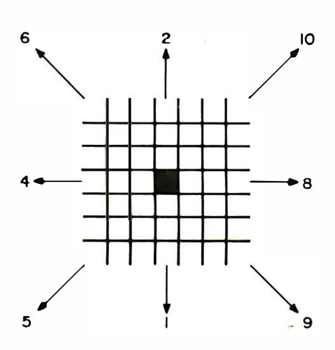
Vector Mode

The bar graph modes are used to draw horizontal and vertical lines. Vector mode allows you to draw lines (called vectors) between any two points. This means slanted lines can be drawn on the screen. Start with PLOT 253, then give the coordinates of the starting position with PLOT X0:PLOT Y0. The next command should be PLOT 242, followed by the coordinates of the end position with PLOT X1:PLOT Y1. (Any variable names can be used; we find these easy to remember.) The program in listing 2 lets you draw vectors on the screen using seven colors in sequence. (Black is not used because it would draw an "invisible" line.)

If you wish to draw lines where the end point of one is the starting point of the next one (as in drawing polygons), you need only use PLOT 253 once. The program in listing 3 draws random vectors in this fashion, making an attractive abstract type of drawing. The output is shown in photo 4.

Incremental Plot

Another submode that can follow PLOT 2 is the PLOT 251 incremental plot, which allows you to move the graphic "point" element (really a small rectangle) by a small "increment" (or step). There are eight directions in which you can move, shown by the arrows in the following diagram:



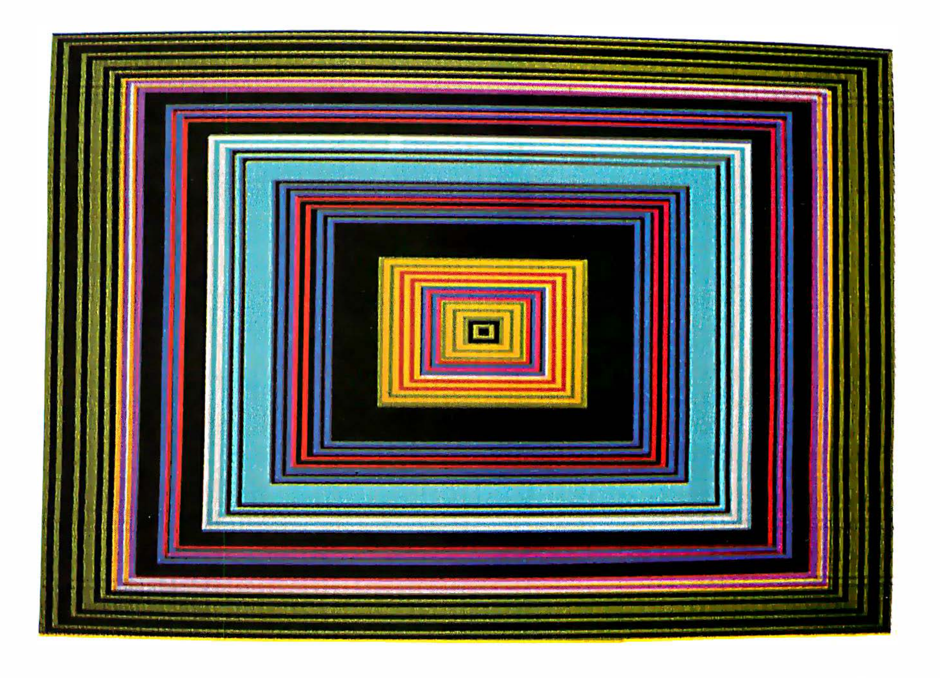


Photo 3. A display of concentric rectangles produced in the bar graph mode.

```
10   PLOT 12:C=0                       'Erase screen
20   C=C+1                             'Start with color code 1
30   IF C > 7 THEN C=1                 'Only allow seven color codes
40   PLOT 6:PLOT C                     'Set the color
50   PRINT"TYPE X0, Y0";
60   INPUT X0, Y0                      'Get starting point
70   PRINT"TYPE X1, Y1";
80   INPUT X1, Y1                      'Get end point
90   PLOT 2                            'Go into plot mode
100  PLOT 253:PLOT X0:PLOT Y0          'Draw vector starting at X0, Y0. . .
110  PLOT 242:PLOT X1:PLOT Y1          '. . .to X1, Y1
120  PLOT 255                          'Exit plot mode
130  GOTO 20                           'Repeat
```

Listing 2: A BASIC program enabling the user to draw vectors on a color video screen using seven colors in sequence.

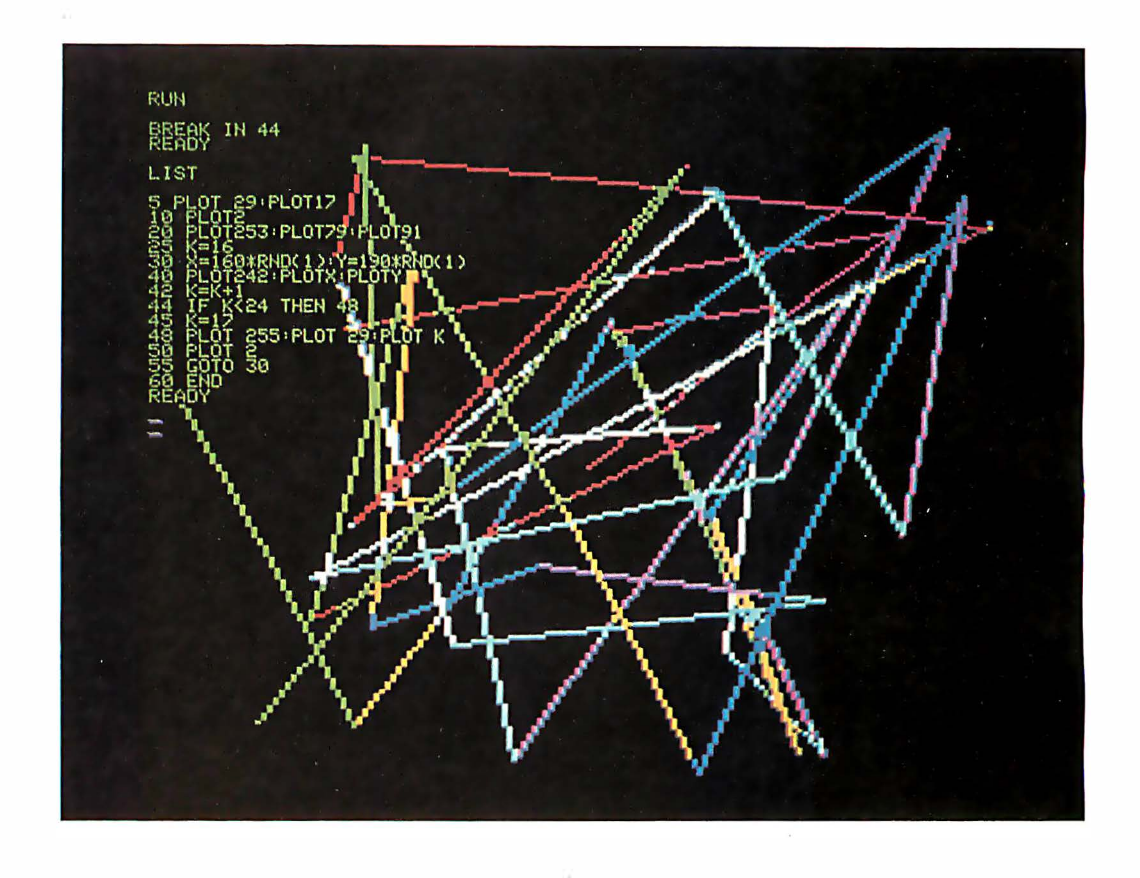
```
10 K=16                                'Initialize color selector
20 PLOT 12:PLOT 2                      'Enter plot mode
30 PLOT 253:PLOT 79:PLOT 91            'Start vector in center
40 K=K+1                               'Select color . . .
50 IF K >23 THEN K=17                  '. . .between 17 and 23
60 PLOT 255:PLOT 29:PLOT K             'Turn on color
70 X=160*RND(1) :Y=190*RND(1)          'Choose random point
80 PLOT 2:PLOT 242:PLOT X:PLOT Y       'Draw vector
90 GOTO 40
```

Listing 3: A BASIC program that draws a chain of random vectors.

```
10   PLOT 12                           'Erase screen
15   PLOT 2:PLOT 80:PLOT 92            'Plot a point in middle of screen
20   FOR C=17 TO 23                    'Select a color
30   PLOT 255:PLOT 29:PLOT C           'Activate color
40   PLOT 2.PLOT 251                   'Go into incremental plot mode
50   E = 2 ↑ INT(4*RND(1) )            'Choose direction
60   FOR K=1 TO 5*RND(1)+5             'Choose number of steps
70   PLOT E                            'Plot in direction E
80   NEXT K                            '     for K steps
90   NEXT C                            'Get next color and direction
100  GOTO 20                           'Repeat the whole cycle
```

Listing 4: A BASIC program to produce a random walk pattern.

Photo 4: A random vectors program display. Color is changed cyclically for each new vector. The listing overwrites some of the vectors because it was done after interrupting the run.



The numbers next to the arrows are "direction codes." A given direction is selected by using the proper direction code in a second PLOT statement. For example, to plot a point in the middle of the screen and then move it one "increment" to the right, use the following instructions:

```
10 PLOT 2:PLOT 80:PLOT 92
20 PLOT 251:PLOT 8
```

PLOT 251 means "increment (move) the point," and PLOT 8 means "to the right." The distance moved is very small (the width of one point).

The next program (see listing 4) uses this feature to produce what is called a random walk pattern. We'll use only the direction codes 1, 2, 4 and 8. These will be generated by the formula

```
E = 2 ↑ INT(4*RND(1))
```

So we randomly get the numbers $2^0=1$, $2^1=2$, $2^2=4$ and $2^3=8$. Our point will randomly "decide" to move down, up, left and right.

To make the pattern even more interesting, we use another random number (from 5 to 9) to decide how many increments (small steps) to take in each direction. We also change colors. The result is a rather striking weave-type color abstraction. (Actually, random walk techniques originated for practical reasons. They are used in solving several types of mathematical and scientific problems that can't be handled by conventional methods.) Line 50 selects a random direction, and the loop 60-80 determines how many increments to take in that direction. The main loop 20-90 repeats the process for seven different colors. The program goes on indefinitely, filling the screen to any density you wish. Photo 5 shows the output of this program after

Photo 5: Output from the random walk program after 20 seconds. When the plotting point "walks off" the edge of the screen, it reappears on the opposite side due to wraparound in the display memory.

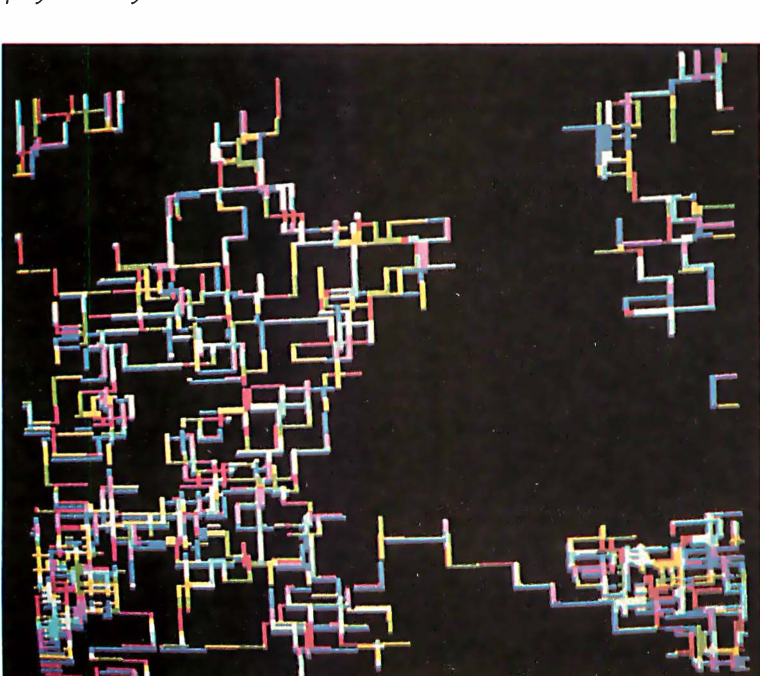




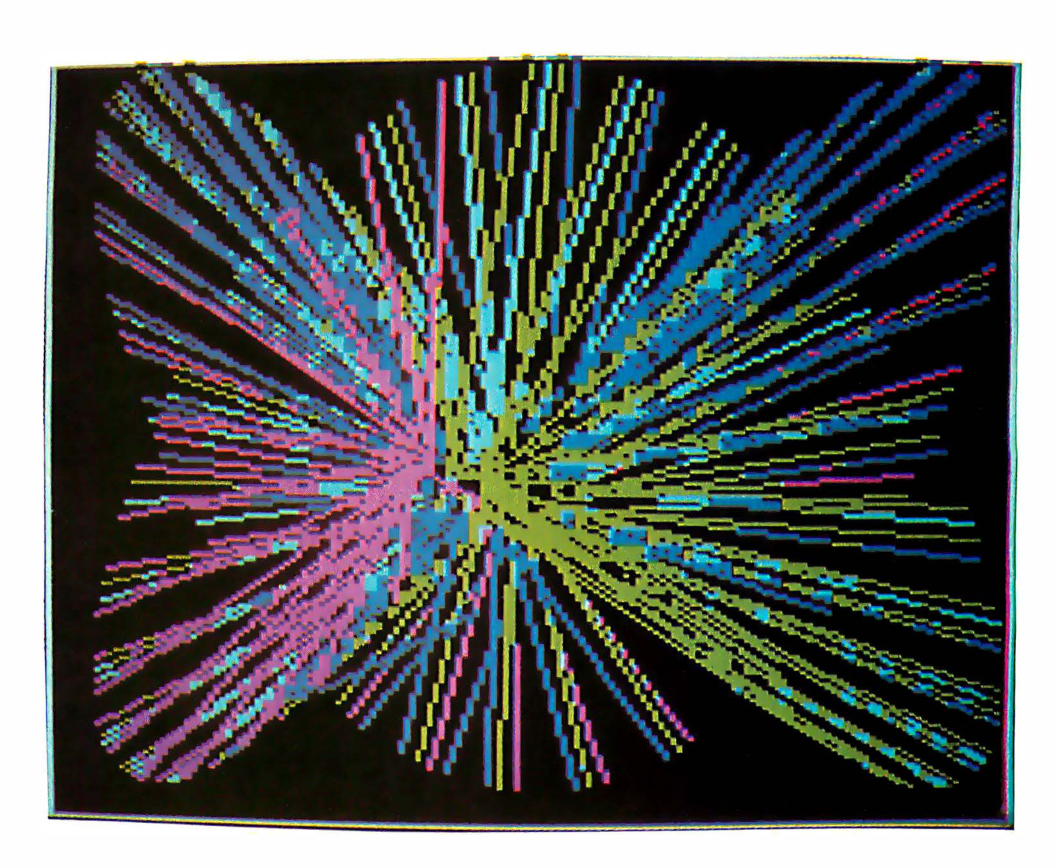
Photo 6: A random walk after 20 minutes. The plotting point moves rapidly, but it frequently overwrites itself. This program can be viewed as a striking way to study random number generators.

20 seconds. Photo 6 shows the output after about 20 minutes. The plotting is rapid, but paths are often retraced.

There are several other subplot modes available, including an incremental vector mode. This has the effect of shifting a vector to a new position very close to the starting position. Since vectors are drawn very rapidly (output to the video display is at 9600 bps), this mode has interesting possibilities for producing simple animation.

A light pen option is also available; it can be used as an input device in developing color graphics. For example, a program in BASIC can be written to accept (X, Y) coordinates from the pen and use these to determine the position of one end of a vector. If the other end of the vector is determined by an algorithm within the same program, the graphic "artist" can interact with the algorithm to produce variations on a design. Photo 7 shows a simple example of this. The outer set of points was determined by an algorithm which generates a 2 by 3 Lissajous figure, while the inner set of points was selected with the light pen. Photo 8 shows the effect of running the same program, having first keyed in a solid blue background. Vectors

Photo 7: A pattern produced with the aid of a light pen. It consists of varicolored vectors; the outer set of end points is determined by a Lissajous figure algorithm. The inner set of end points is selected with a light pen.



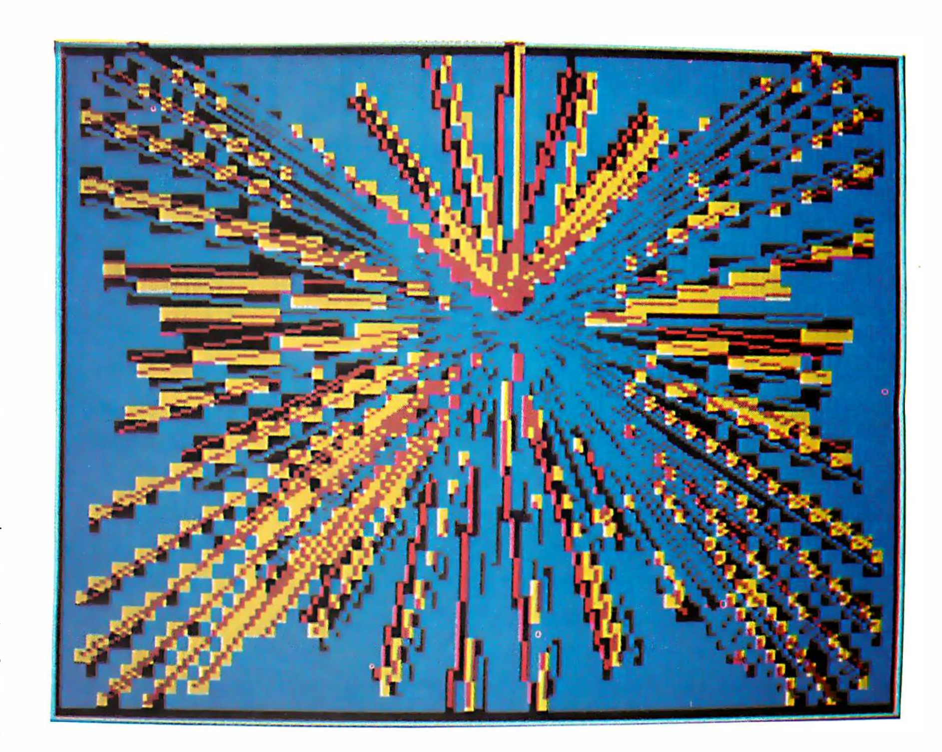


Photo 8: A pattern produced in the same manner as that of photo 7, except that the background color has first been set to blue. Background was reset to black to draw some of the vectors, and to blue for others. The artist used the light pen to draw a sprinkling of "blue on blue" vectors over the final pattern to produce a "burst" effect.

were drawn in "color-on-black" and in "color-on-blue" modes. A general program for experimenting with the light pen in this manner is given in the book *BASIC and the Personal Computer* (Addison-Wesley, Reading MA 01867).

Given the value of output in the form of dynamic as well as color graphics, and the complex ideas which can be programmed in Compucolor BASIC, the Compucolor 8051 is quite an interesting machine. Its design invites explorations well beyond those described in this brief introduction.■

Circle 286 on inquiry card.

Basic systems for personal computing

If you are just getting into personal computing and are looking for a starter system, you have two choices: a computer kit with RAM memory only or a fully assembled computer with BASIC-in-ROM. From reading this magazine and talking to computer buffs it should be obvious that it is desirable to have a computer capable of communicating in the programming language BASIC. This language allows you to instruct the computer in English-like phrases and to use any of the thousands of standard programs written in BASIC (there are probably several in this magazine).

If you purchase a (RAM-only) computer kit you will have to buy additional RAM (4K to 8K), a terminal, and cassette interface for a total cost of about $1000 to run BASIC after you get the kit together and working. Your reward for this endeavor will be a wait of about 15 minutes every time you turn the computer on just to load BASIC into the machine!

Your other alternative is a BASIC-in-ROM computer. These machines have BASIC built in so that it is there whenever the computer is turned on. BASIC-in-ROM computers are also usually fully assembled and cost far less than the RAM-only kits because they are mass-produced by the thousands.

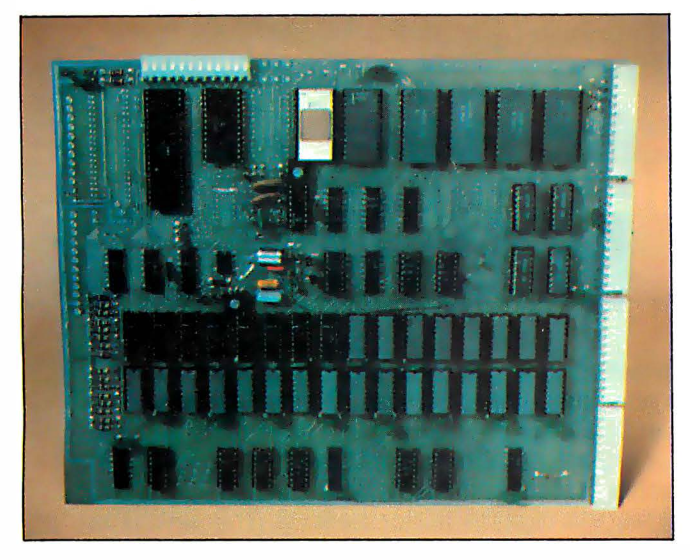
But, you must be careful when selecting a BASIC-in-ROM computer. Some models do not have full-feature BASIC. Instead they have Tiny BASIC or 4K BASIC which cannot run most of the standard BASIC programs available. Still others have other shortcomings such as a small calculator-style keyboard which makes program entry difficult, or most important, lack of expansion capability, preventing the computer from growing with you.

Ohio Scientific offers you a line of expandable computers with full-feature 8K BASIC-in-ROM. They all come fully assembled and tested, but give you the option of economizing by supplying the simple things — power supply, keyboard and TV, if desired, so that you get the most computer power for your dollar.

Compare Ohio Scientific's $298 BASIC-in-ROM Model 500 Board (1MHz clock), which has our Version 3.3 BASIC, against other small computers, as in the independent article "BASIC Timing Comparisons" (Kilobaud, Oct. 1977, p. 23). In this test, the Model 500 excelled over all our personal computing competitors, and was second in performance only to our Challenger disk systems, compared against twenty-eight other computer systems. And the Model 500 is our lowest-cost machine! Our larger models are even more dramatic in a comparison with any competitive models.

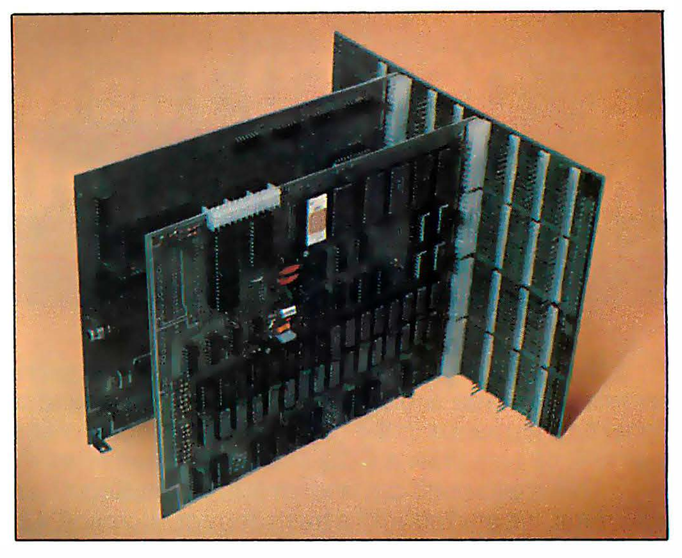
Having the fastest full-feature BASIC ROMs certainly isn't the only criterion necessary for a superior computer system, but it sure helps. Ohio Scientific offers all the other features necessary, including a full line of computer accessories complete with 15 accessory boards available in over 40 configurations. Many Ohio Scientific accessories are so innovative that no one else in the industry has them — such as dual port memory boards, multiprocessing CPU's and big disks.

Ohio Scientific has other unique features for the personal computerist. For instance, there is Ohio Scientific's *Small Systems Journal,* published bi-monthly, a full magazine aimed specifically at the owners of Ohio Scientific computers. If you are looking for a personal computer, be sure to look carefully at Ohio Scientific. We think you will find that we have the system for you.



Model 500 Board

A full 8K BASIC-in-ROM computer on a board. This unit contains a 6502 microprocessor with our powerful 8K BASIC-in-ROM, 4K of RAM memory, and a serial port which can be jumpered for 20ma current loop or RS-232. The board can be plugged into any standard OSI-backplane and expanded by our full line of accessory boards. The user must simply supply +5V and −9V power and the serial terminal to be up and running in BASIC.
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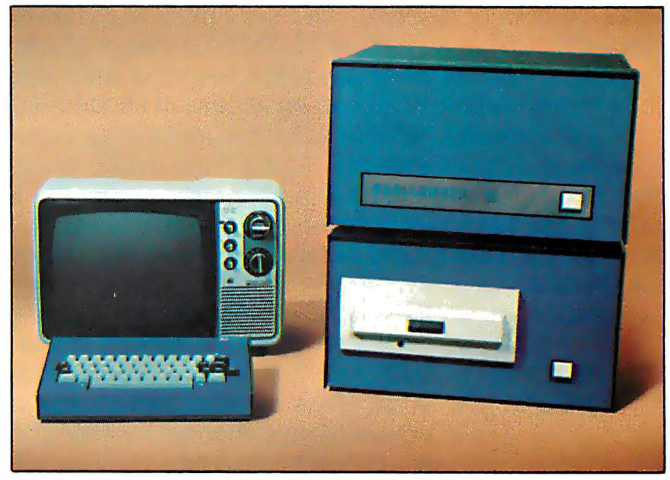
Super Kit

An ideal starter computer system. The Super Kit includes a Model 500 CPU Board with 8K BASIC in ROM, CPU, and 4K of RAM, full buffering for expansion, an eight-slot backplane board, and a Model 440 Video I/O Board. Model 440 provides full CRT functions when connected to a video monitor or modified television set and a standard ASCII keyboard. The user must simply provide +5V and −9V power, an ASCII keyboard, and a modified television set or monitor to have a full computer system with 8K BASIC-in-ROM, 4K user space and a CRT terminal with scrolling.
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Challenger II• P

Our very popular fully packaged BASIC-in-ROM computer. Challenger IIP contains the Model 500 CPU Board with 4K of RAM, our new 540 32x64 character video display, keyboard and complete audio cassette interface. The unit also has internal power supplies and a four-slot backplane with two open slots for expansion. The user has only to connect a monitor or modified television set to its output, and he is ready to program in BASIC. To store programs and data files, he needs only to connect a conventional audio cassette recorder to the built-in audio cassette interface. The unit is fully assembled and ready to go.
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Challenger II Disk Systems

The ultimate in personal computing offered by Ohio Scientific is the Challenger II system with single- or dual-drive full-sized floppy disk. Each floppy stores 250,000 characters. The Challenger II is available as a video system with keyboard so that all the user needs is a television or monitor for operation; or as a serial version where the user must supply his own terminal. Challenger II disk systems automatically load in BASIC and now have an extensive library of high-performance programs. The programs are ideal for the advanced hobbyist, educational users, industrial development and small business applications. Challenger II disk systems are very economical. For instance, a 16K disk system with 250,000 bytes of disk storage starts at under **$2000.00**



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System design goals: Create a simple, concise crash proof operating system which is easy for business programmers to utilize and simple for office workers (and other non-computerists) to use. The system *must* have the highest performance in the microcomputer industry and must be able to support present day floppy and hard disks as well as tomorrow's CCD and bubble memories *without any user program modifications.*

This may sound outlandish but we developed just such a system and here's how:

First, we started with a fresh copy of Microsoft's super fast 9½ digit BASIC for the 6502. (This BASIC out benchmarks every other microcomputer BASIC using the 7 Kilobaud benchmarks except for our own ultra fast 6 digit BASIC.)

We knew that all operating system commands and features should be an integral part of this BASIC language so we put them right in the BASIC itself. This means that all OS features can be accessed in the immediate or command mode and as part of BASIC programs. All syntax such as file names can be literal strings or BASIC variables.

We started with some simple but powerful extensions to BASIC to make the business system programmer happy– like $L, $R, INPUT #(D), and PRINT #(D). $L and $R are PRINT subcommands which automatically output numeric data in dollars and whole cents in neat columns just like "PRINT USING" only simpler and quicker.

The optional # specifier in LIST, INPUT and PRINT statements allows the user to route I/O directly to the console, 16 RS-232 ports, a cassette port, RS-232 and parallel printer ports and word processing printers, not to mention video displays and parallel keyboards.

We then added a continuous memory file system—the real achievement of OS-65U. This file system has no tracks, sectors or records. The user simply allocates storage capacity to each file when he creates it. (On a CD-74 Hard Disk this can be over 72,000,000 bytes or characters.) The user can then directly address every entry in the file with no awareness of any block, sector or track structures. Data files can simultaneously contain strings and pure numeric data. Files can be accessed sequentially *and* randomly.

Data files are handled with standard syntax including OPEN "File", CLOSE (File), PRINT % (File) and INPUT % (File) and the very special INDEX (File). INDEX is a special BASIC variable/function which specifies the file address of the next entry to be input or output to that file. If you leave it alone, it operates sequentially. However, you can change it at any time to force a random access. This remarkable function can be on either side of a BASIC equation and can take on any value within the storage range of an opened file. For example, all of the following are legal in OS-65U:

```
INDEX (1)  =  INDEX(1)  +  10  (Causes 10 characters to be skipped)
        B  =  INDEX (1)  (Sets B = current index)
INDEX (3)  =  INDEX(8)  /2 (Equates two file positions, useful in sorts and merges)
INDEX (5)  =  A*50  (Sets up a random access on an array with 50 character elements)
```

Where (N) is a channel number or shorthand notation for an open file, and is assigned by the OPEN command.

This may seem exotic but it is really super simple and incredibly powerful. Besides your files always automatically revert to simple sequential operation if you choose to ignore indexes.

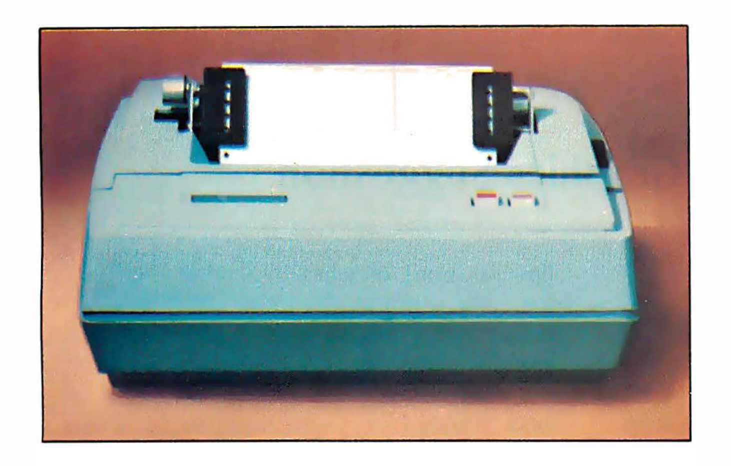
And, finally, for those of you who would really hate to give up plain old sequential files, we added a FIND command. FIND searches for up to a 32 character string with optional "don't care" characters and will automatically scan any file from the beginning or other specified index. The FIND command is implemented in straight line page zero 6502 code (the fastest programming technique on the fastest micro) and searches files at over 250,000 bits per second.

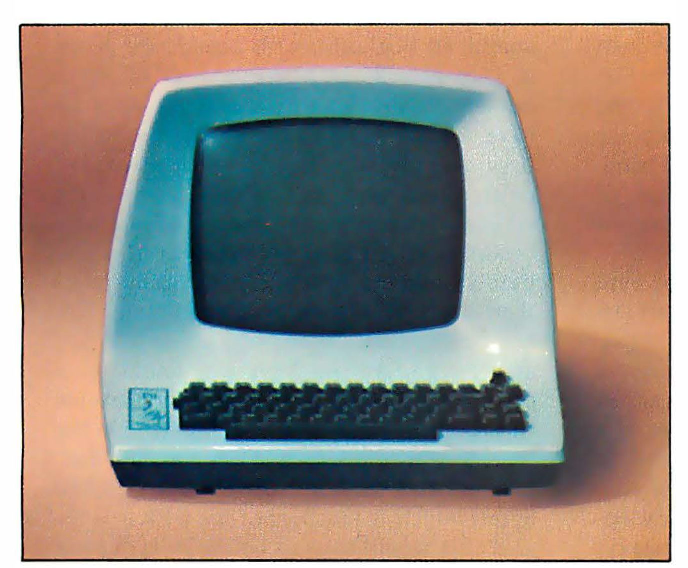
Only three statements are needed to support a sequential file in a BASIC program; only four to support a random file. A mere seven statements are required to use an indexed sequential file system as part of a program!

A Benchmark: A Challenger III equipped with a CD-74 running OS-65U can access any account entry in a 500 account one million byte randomly ordered ledger file by an alphabetic key string up to 32 characters long in less than 40 milliseconds (typically) using a simple two level ISAM file structure supported by a total program only 10 statements long. That's performance!

OS-65U also hosts multilevel passwords, elaborate error checking, programmable error recovery and end user niceties like warnings and automatic recovery when an "off" or non-existent peripheral is accessed. Programs and files in OS-65U can be fully secured so that they cannot be listed, copied or even accessed if desired.

OS-65U is available now for use on any Ohio Scientific floppy or hard disk based computer with 32K of RAM or more. At $199, it's quite possibly the best computer investment you'll ever make.







The Challenger III System

- Designed for small business computing.
- Uses the 510 triple processor CPU Board, runs 6502, 6800, 8080 and Z-80 programs.
- Available with up to 1 Megabyte of RAM memory; high reliability static RAM is standard; low-cost dynamic RAM is optional.
- Single- or dual-drive floppy disks store 250,000 characters per surface — 3 to 4 times the storage of mini-floppies.
- Supports our ultra-fast 6-digit BASIC (see "BASIC Timing Comparisons," Kilobaud, Oct. 1977, p. 23, where Ohio Scientific out-benchmarks all of our competitors) and our new super-fast 9-digit business BASIC.
- Powerful operating systems support all standard I/O ports including multiple terminals, line printers, video display and disk.
- Disk supports: sequential, random and index sequential files.
- Applications software, including:
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- Two factory-supported terminal options and two factory-supported line printer options.
- Optional 74-Megabyte hard disk for $6000. Reel-to-reel mag tape coming soon.
- Optional 16-user operating system with time share and distributed processing capabilities.
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- Leasing programs and maintenance contracts available through many dealers. Optional nationwide field service coming soon.
- Challenger III systems have extremely high performance-to-cost ratios. For example, a system complete with triple processor CPU, 32K bytes of static RAM, a serial I/O port, dual drive floppy disks (500K bytes of on-line storage), fully assembled, plus DOS, BASIC and a demonstration program library costs $3590 fully assembled.

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Technical Forum

A Raster Scan Graphics Suggestion

Tello D Adams
619 Woodhaven Pl
Richardson TX 75080

In reference to your editorial (October 1977 BYTE, page 6) you seem to have overlooked a pertinent color refresh storage method. While a 256 by 256 matrix is great if you want to create a 256 square checkerboard, most graphics (including cartoons) don't look that way; therefore, storage for every picture element is a waste of bandwidth. Most graphics consist of areas of color, usually with a limited number of changes over the screen width.

Let us presume that a representative byte consists of four bits of color information (16 colors) and four bits of intensity data (grey scale = 16). A raster scan system is *not* a series of random events. The beam position can be predicted at all times, therefore, if a clock driven 256 counter (eight bits) is provided, the horizontal position of the beam is uniquely defined. The game now becomes one in which the beginning address on a line (eight bits) and the color and intensity information (eight bits) from that point to the next change is stored (parallel 16 bit or two bytes if your access is fast enough) in sequence in memory. Each 16 bit word is pulled from memory and stored in two 8 bit registers. When the counter (horizontal line position) matches the address register, the color and intensity information is transferred into a driving register which holds it and drives the video conversion circuits until the next change. This event also causes the next double byte to be retrieved from the memory and loaded into the "standby register." The driving register could also be combined (logically) with a character generator to provide an interesting set of alphanumerics. Now let's look and see what we have got. We need a sync signal to mark the beginning of the frame, but no line counter, unless you want to digitally control the vertical retrace, as a given address only occurs once per line. (But you do need one byte of address which is numerically larger than the first address of the next line. This can be an actual "used" number or a "fake" at n = 225.) We use only one double byte per color or intensity *change.* If you assume an *average* of ten changes per line (and in the "cartoon" world that is a lot) and 256 lines, that equates to 2,560 double bytes (5,120 bytes) which is far short of the 64 K + bytes (7.8%) it would take to define every picture element, yet 256 by 256 *resolution* is still achieved (information and resolution are *not* the same). This would seem to provide one practical solution to the high resolution color graphics problem for small users, and is instantly expandable as more memory becomes available.■

Technical Forum is a feature intended as an interactive dialog on the technology of personal computing. The subject matter is open-ended, and the intent is to foster discussion and communication among readers of BYTE. We ask that all correspondents supply their full names and addresses to be printed with their commentaries. We also ask that correspondents supply their telephone numbers, which will be printed unless we are explicitly asked to omit them.

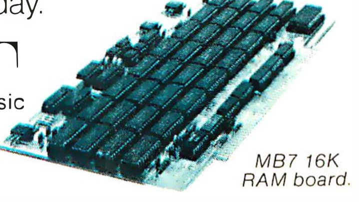
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UCSD PASCAL: A (Nearly) Machine Independent Software System

(for Microcomputers and Minicomputers)

Kenneth L Bowles
Professor, Director
Institute for Information Systems
University of California San Diego
La Jolla CA 92093

Languages Forum is a feature which is intended as an interactive dialog about the design and implementation of languages for personal computing. Statements and opinions submitted to this forum can be on any subject relevant to its purpose of fostering discussion and communication among BYTE readers on the subject of languages. We ask that all correspondents supply their full names and addresses to be printed with their commentaries. We also ask that correspondents supply their telephone numbers, which will be printed unless we are explicitly asked to omit them.

Overview

This article describes a complete interactive software system which can operate virtually without change on many different microcomputers and minicomputers. Because the semiconductor industry is evolving new equipment very fast, it is becoming a practical necessity to have machine independent software to prevent rapid obsolescence of large application programs. The software described here has been developed at the University of California San Diego (UCSD), and is available to anyone for a $200 subscription fee. This article presents an appeal to readers of BYTE for help to bring about a true community-wide software system for business, educational and other professional users of small computer systems. Help is needed from the user community, since the manufacturers have so far avoided standardizing software except as regards some aspects of programming languages. For single user microcomputers, it appears to be far more practical to *standardize the entire software system* than the language processor alone!

The Software System

UCSD PASCAL is a complete interactive software system for small computers, yet it offers many features normally found only on medium and large scale machines. It is designed to operate, with minimal adaptation, on most microcomputers or minicomputers based on 8 bit bytes or 16 bit words. Supported versions are now available for use on machines based on the Digital Equipment LSI-11 or other PDP-11 processors, and on the 8080 and Z-80 microprocessors. Having first been sent to users in August 1977, the system is in use on approximately 60 mainframes using these processors (as of mid February 1978), and the list of both users and processors has started to grow rapidly. Versions not yet supported by the Project are operating, or nearly operating, on four other processors (General Automation 440, Univac V75, Nanodata QM-1, National Semiconductor PACE). The UCSD PASCAL Project is discussing arrangements with various manufacturers whereby supported versions can be released for most other popular microprocessors, and additional inquiries would be welcomed.

The system is written almost entirely in the PASCAL programming language, extended for system programming and for disk based interactive applications. Far more than a simple *compiler* for PASCAL, it should be viewed as a complete and fully integrated system which is self-maintaining, and generally independent of software from any other source. The system operates in a small pseudomachine (interpreter) which can be written in the native machine language of conventional processors, or can be microprogrammed on machines which provide that capability. The object code processed by the PASCAL pseudomachine is compressed relative to conventional object code, and consumes roughly one third to one half as much space as the native object code of most present day processors. A feature to be implemented soon will allow mixing PASCAL pseudocode routines, for efficient use of memory, with native code routines, for fast processing.

The system is the product of a growing project team, and is evolving rapidly in an upward compatible way. As of early 1978, the system represents the equivalent of about 15 full-time years of programming and design effort. Major components of the

Continued on page 170

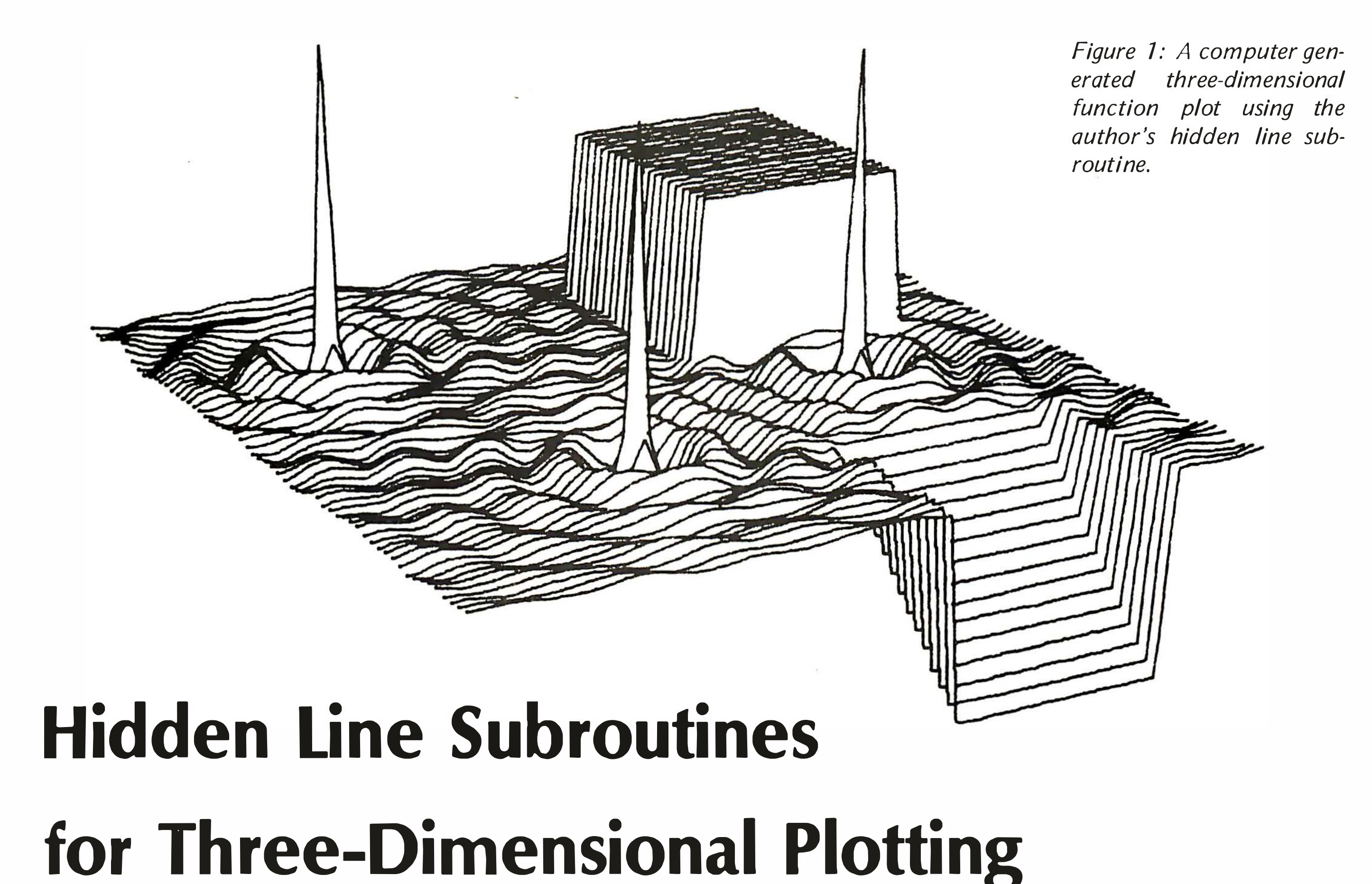


Figure 1: A computer generated three-dimensional function plot using the author's hidden line subroutine.

Hidden Line Subroutines for Three-Dimensional Plotting

Mark Gottlieb
4342 Sunset Beach Dr NW
Olympia WA 98502

A hidden line subroutine is used to eliminate lines which are behind surfaces and which in real life one would not be able to see in a computer generated plot of a solid object in two dimensions. A hidden line subroutine makes the final picture more realistic.

A three-dimensional Cartesian function is a function such as

$$F(x,y) = 4x\cos(3y) + 1/e^{x}$$

where the value for the z coordinate is a function of both X and Y.

This article considers the various steps necessary for a hidden line routine that handles functions of this kind. The algorithm will *not* work for functions plotted in spherical coordinates or for complex three-dimensional figures such as a house.

The hidden line subroutine should be written in a general form so that the user can attach the subroutine to any appropriate program without having to rewrite it.

First, one must have a program that generates the X and Y values that the hidden line subroutine will operate on. Briefly, this involves a program to generate an X and a Y FOR NEXT loop; generate a Z value; rotate to get a new (x',y',z'); scale; put through a perspective function and come out with an (x,y) point. This is the point on the screen (or paper) to which one would normally draw a line. However, we now take this (x,y) point and GOSUB to our hidden line subroutine.

Let us first draw a function of this kind without hiding any lines (see figure 2). Note that one point seems to ruin the appearance of the graph because the viewer sees immediately that a surface is being formed. When a point goes "behind" the small mound, the subjective feeling is that it should be hidden. We need a rule that will handle all points that should be hidden and leave other points alone.

One difference between this point and all the previous points is that it is lower (along the Y axis) than the corresponding point in the previous line. "Corresponding" here means the *same X value.* Thus, our rule states that if for any point (x,y), the Y value is lower than any previous Y value for the same X value, it should be hidden. To do this, we must save the necessary values; for the above rule, we need to know the highest valued Y for every X.

Let us assume the screen has a resolution of 1024 along the X axis and 800 along the Y axis (such as in the case of the Textronix

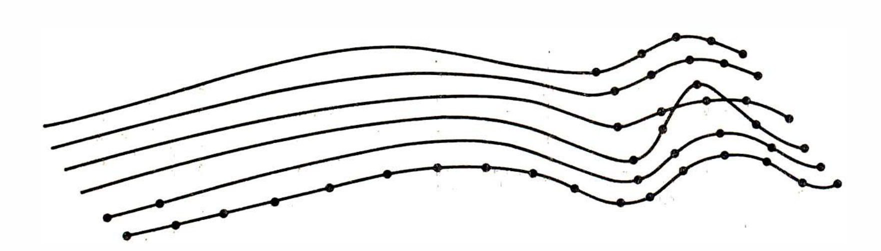


Figure 2: The first crude plot function shows problems encountered when no hidden line algorithm is used. The subroutine would hide that portion of the fourth line from the front that "goes behind" the high point in front of it.

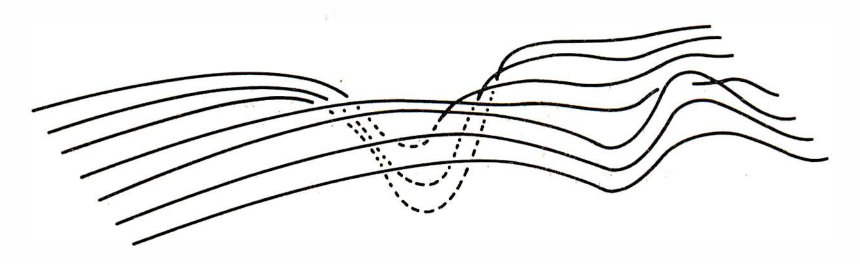


Figure 3: In this case the algorithm has correctly hidden some points but has failed to show others which emerge at the bottom of the plot.

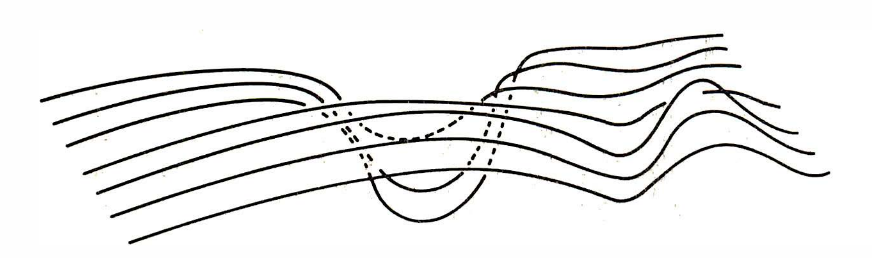


Figure 4: Improved algorithm reveals the bottom of the curve as a series of solid lines (compare with figure 3).

A Note About the BASIC Employed in These Examples:

The BASIC employed in these examples is the interpreter available with the author's computer. Most features are similar to a typical extended *BASIC which includes matrix operations (MAT keyword). As noted in text, the file oriented operations which are used to initialize the matrix B can be replaced by a FOR ... NEXT loop at lines 310 and 320 in listing 6. (Lines 130 and 140 would then be deleted.)*

```
5505   U6=SGN(X-X9)
5510   IF U6=0 THEN 5535
5515   FOR U7=X9 TO X STEP U6
5520      S8=Y9+S9*(U7-X9),B[U7,2]=B[U7,2] MIN S8,B[U7,1]=B[U7,1] MAX S8
5530   NEXT U7
5535   RETURN
```

Listing 1: A BASIC program used to calculate points between the endpoints of a line segment for plotting purposes.

4013 graphics terminal). Thus, we have 1024 possible X locations. But we need to know only the highest valued Y for each X. This means that if we have a 1 by 1024 matrix we can store the highest valued Y in the corresponding X location. We can keep our matrix updated with the following BASIC statement:

100 B(X,1) = B(X,1) MAX Y

This statement always keeps the matrix full of the highest valued Y for each X location.

In order to implement our rule in the hidden line program, we need a check such as:

If Y < B(x,1)
Then *don't draw this line.*

Implementing what is already known, the graph might look like the one in figure 3.

The program hides all of the lines shown as broken lines because all the Y values for those X values are less than the highest Y value for that X value. However, we see that we would like to have seen the part of the dip which comes out beneath the graph. In other words, we want our graph to look like the one in figure 4.

Instead of hiding all the lines whose Y value is less than the highest Y value for that particular X, we should say "Hide all lines whose Y value is less than the highest Y and greater than the lowest Y value for that particular X." This involves storing the lowest Y value, also. We do this by using the matrix with dimensions (1024,2). In column 1 we store the highest Y value and in column 2 the lowest Y value for that X. The matrix can be kept up-to-date this way:

B(X,1) = B(X,1) MAX Y
B(X,2) = B(X,2) MIN Y

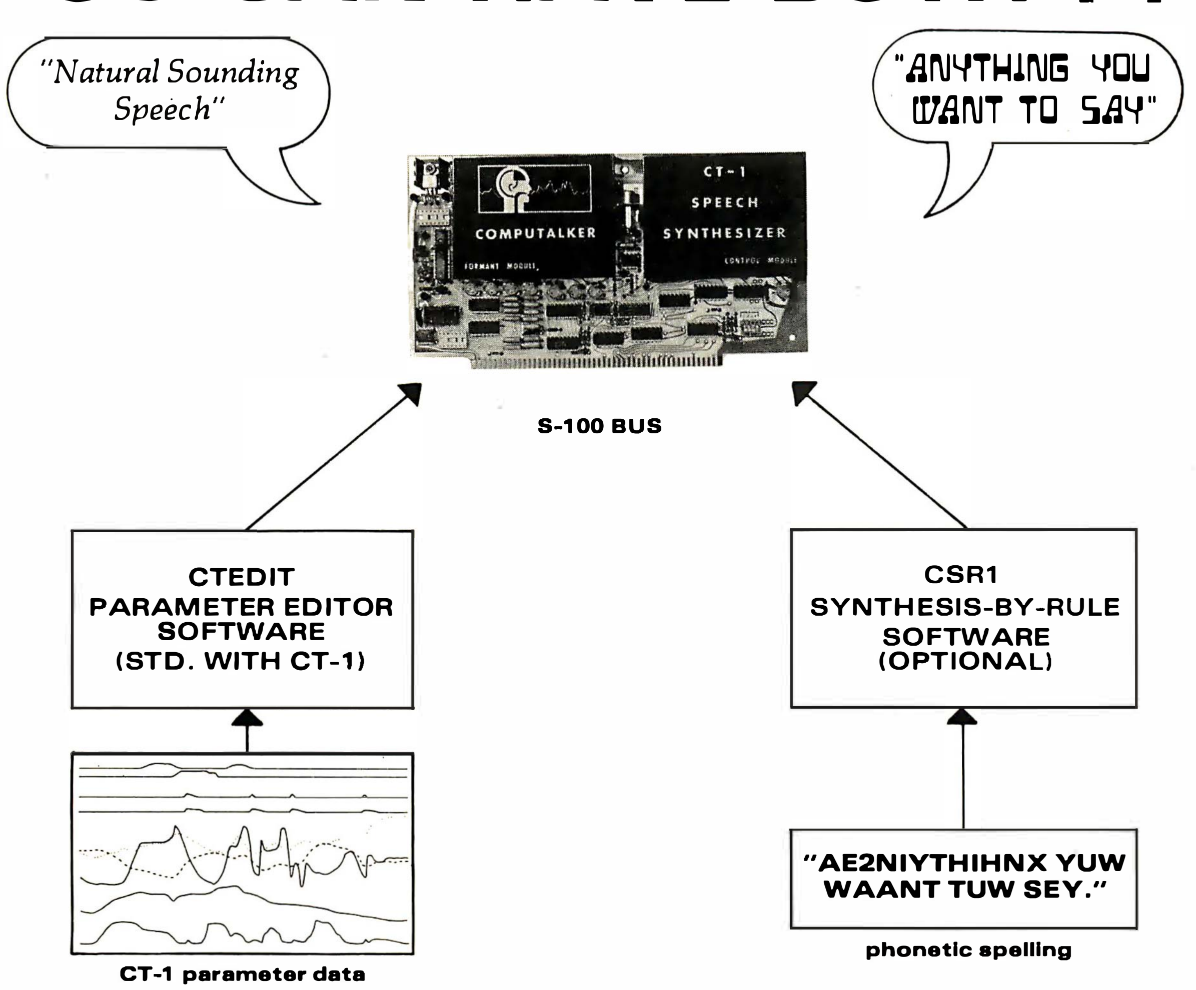
This statement keeps the matrix full of the highest and the lowest valued Y for each X location. Thus, the new check for the hidden line routine looks like this:

If Y < B(X,1) AND Y > B(X,2)
Then *don't draw.*

One small technical problem arises which is easily solved. We need to solve for only two points in order to get a line between them, but our (1024,2) matrix has not been told what is between these two points. Thus, for each new point solved, we must go through the matrix, starting from the X value where we last left off, and fill in the Y values for each of these new Xs until we get to the X value of our new point (x,y).

This process involves solving the equation for a straight line given the two points and then filling in the Y values for each X

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Figure 5: Plot made without the intersection routine. Incorrect intersecting lines are caused when line segments which are partly visible and partly hidden are plotted.

along that line for our matrix. This routine is called upon almost every time a new point is generated, and, therefore, is executed many times. This is the one step that makes this method of hidden line processing slow, and thus should be made as condensed as possible. A suggested routine is shown in listing 1. In this routine, U6 causes the FOR NEXT loop to go forward or backward depending on where X is in relation to X9. X9 and Y9 are set equal to the previous points throughout the program. U7 becomes the X value for each point along the line and S8 the corresponding Y value. S9 is the slope of the line and is determined earlier in the subroutine. Matrix B is the 1024 by 2 matrix for storing the high and low Ys.

One small item which must not be overlooked is that the initial values of the 1024 by 2 matrix elements must be set. Suppose we initially set each element to 0. While drawing the first line, suppose the first point is (300,200). When the program executes the line which reads

```
100 B(X,1) = B(X,1) MAX Y
    B(X,2) = B(X,2) MIN Y
```

element B(300,1) will take the MAX of 0 and 200 which is 200; this is correct. However, element B(300,2) will take the MIN of 0 and 200 which is 0. This is incorrect; the desired answer is 200. We can solve the problem by filling all of the elements in the second column with the highest value we might need, 800 in this case.

One way (used in my program) to fill the first column with 0s and the second with 800s is to use a file. The initial conditions are read from the file onto the matrix at the beginning of each program. Another way, of course, would be to employ a FOR ... NEXT loop.

The few techniques learned so far form a good basis for a hidden line subroutine. Plotting a function with a hidden line subroutine and incorporating what has been determined so far gives a graph like the one shown in figure 4. An outline for the hidden line subroutine would be similar to this:

- If Y < B(X, 1) and Y > B(X, 2)
  Then *don't draw.*
  Otherwise draw.
- *Fill in points in matrix.*
- *Return to main program.*

Figure 4 looks respectable; at least the right lines are hidden. However, something is not quite right. When we need to hide a point, we cannot simply draw a line to that point. This leads to the problem seen in the graph; the lines do not meet the surface of the graph when they go behind; when coming out, they start emerging before they are completely clear of the surface. Obviously, some improvement on our hidden line subroutine is needed.

We need an algorithm to find the intersection. When a point lies behind the surface, we must find a new point on the

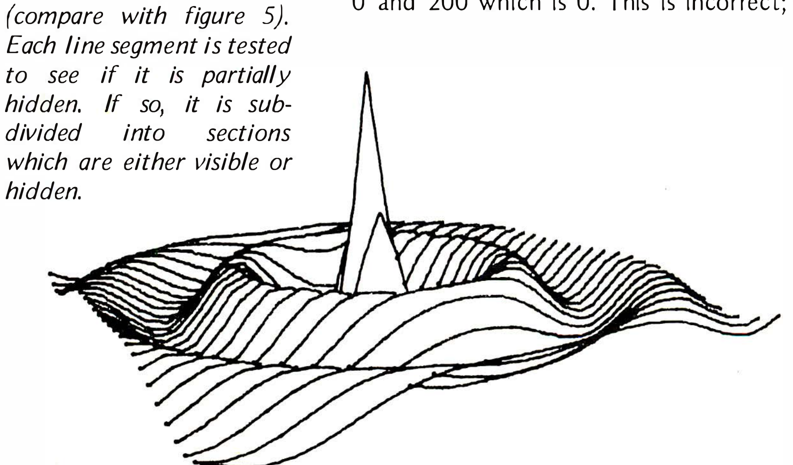


Figure 6: Plot made using the intersection routine (compare with figure 5). Each line segment is tested to see if it is partially hidden. If so, it is subdivided into sections which are either visible or hidden.

```
5205    S7=X-X9,U2=0,X1=X9,U1=1
5210    UNTIL U1>128 DO
5215        U1=U1*2
5220        IF U2 THEN 5235
5225        X1=X1+S7/U1
5230        GOTO 5240
5235        X1=X1-S7/U1
5240        Y7=S9*(X1-X9)+Y9
5245        IF U3 THEN 5456
5250        IF Y9>B[X9,2] THEN 5270
5255        IF Y7>B[X1,2] THEN U2=1
5260        IF Y7<B[X1,2] THEN U2=0
5265        GOTO 5280
5270        IF Y7<B[X1,1] THEN U2=1
5275        IF Y7>B[X1,1] THEN U2=0
5280    DOEND
5285    X5=X,Y5=Y
5290    X=X1,Y=Y7
5455    REM ** FOR U3=1:COMING OUT ***
5456    IF Y>B[X,1] THEN 5460
5457    IF Y7<B[X1,2] THEN U2=1
5458    IF Y7>B[X1,2] THEN U2=0
5459    GOTO 5280
5460    IF Y7>B[X1,1] THEN U2=1
5465    IF Y7<B[X1,1] THEN U2=0
5470    GOTO 5280
```

Listing 2: A BASIC routine that searches for intersections between line segments.

surface of the graph. If we draw a line to a point that should be hidden, we will intersect the surface at this new point which we are trying to locate: the point of intersection. This becomes tricky. The basic procedures necessary to determine the point of intersection are as follows:

- Find the equation for the line which passes through the previous point and the new point behind the surface.
- Step along this line from the old X value to the new X value until we find an X where the Y for that X is the same (within one point of resolution) as the highest (or lowest) Y for that same X. This is the intersection point to which we draw to intersect the surface, or from which we start drawing when coming from behind the surface.

Suppose the point outside of the surface is (505,200) and the new point which goes behind the surface is (575,188). If we step along the line joining them in the X direction, from X = 505 to X = 575, it could take up to 70 steps until the intersection point is found.

A much more elegant and time saving approach is to perform a "binary search" along the line to find the intersection point. For the previous example in which there were 70 steps, we could get to within one point of resolution from the point of intersection in seven steps. I go through the binary search method eight times to accommodate longer line segments.

Listing 2 shows the segment of my hidden line subroutine that searches for the intersection point. U1 is a binary loop; U2 tells whether to go forward or backward along the line segment whose length is S7; X1 is the new X location along the line segment as the search continues; Y7 is the solution to the line equation between the two points at the new X value X1; and U3 calls a further nested subroutine if one is trying to find the intersection point while coming out from behind the surface. Finally, after the program executes the loop eight times, X1 and Y7 are the coordinates of the intersection point (X1,Y7). Figures 5 and 6 show the before and after effects of the intersection routine.

Figures 7 and 8 show what happens to a graph with and without a process called "left and right side fill-in." The edges of the graph in figure 8 appear messy. This is because on the left edge, for example, when a line comes into the preceding left edge, it does not appear to intersect it; instead it goes a bit too far. This can be seen with the aid of the dotted line. The problem is solved by adding an imaginary dotted line into the matrix of 1024 by 2. Although we do not draw the edge lines on the screen which we *could* do, we "draw" them into the matrix. Thus, when a line is about to intersect with an edge, it will have an imaginary boundary in the matrix with which to intersect.

The matrix fill-in is accomplished by taking the point at the beginning of a new line and the point for the beginning of the previous line and calling them (X,Y) and

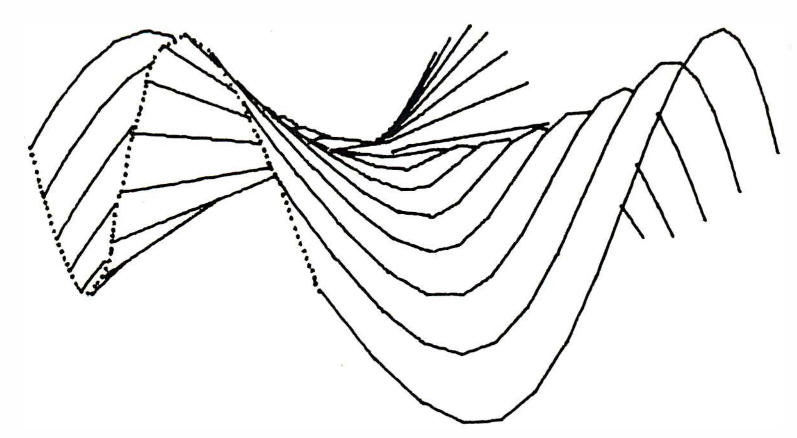


Figure 7: Graph made with "left and right side fill-in." The term refers to an imaginary "edge" at the borders of the surface (shown in dotted lines). This edge enables the algorithm to accurately handle lines drawn near the edges.

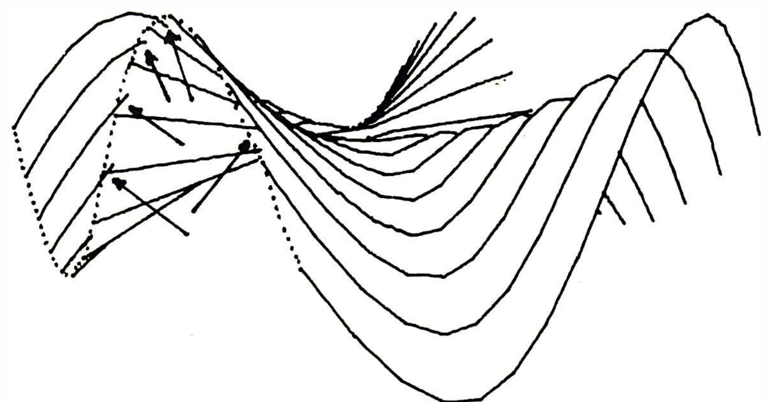


Figure 8: Graph made without the "left and right side fill-in" feature in the algorithm. In this case the routine cannot accurately handle intersections at the edges of the surface (see arrows).

```
5600  REM ** FILL IN LEFT SIDE **
5610  IF X4#-1 THEN GOTO 5640
5620  X4=X,Y4=Y
5630  RETURN
5640  X8=X9,Y8=Y9
5650  X9=X4,Y9=Y4
5660  S9=(Y-Y9)/(X-X9)
5670  GOSUB 5500
5680  X9=X8,Y9=Y8
5690  GOTO 5620
5700  REM ** FILL IN RIGHT SIDE **
5710  IF X3#-1 THEN 5740
5720  X3=X,Y3=Y
5730  RETURN
5740  X8=X9,Y8=Y9
5750  X9=X3,Y9=Y3
5760  S9=(Y-Y9)/(X-X9)
5770  GOSUB 5500
5780  X9=X8,Y9=Y8
5790  GOTO 5720
```

Listing 3: Two routines used to "fill in" the left and right sides of the graph so that no line intersections occur (see figures 7 and 8).

```
300    FOR B=0 TO 1
302       X3=Y3=X4=Y4=-1
303       READ #2,1
305       MAT READ #2;B
310       FOR T=-E TO E STEP E/K
320          FOR G=-E TO E STEP E/K
330             U9=G
340             IF B=0 THEN 370
350             A[1,1]=T
355             A[1,2]=G
360             A[1,3]=T*G*(T*T-G*G)/(T*T+G*G)
365             GOTO 400
370             A[1,1]=G
380             A[1,2]=T
390             A[1,3]=T*G*(G*G-T*T)/(G*G+T*T)
400             MAT C=A*Q
410             X=FNP(C[1,1]*300/E)+512
420             Y=FNP(C[1,2]*300/E)+400
430             GOSUB 5000
440          NEXT G
450       NEXT T
455    NEXT B
```

Listing 4: A routine to create crosshatched plots.

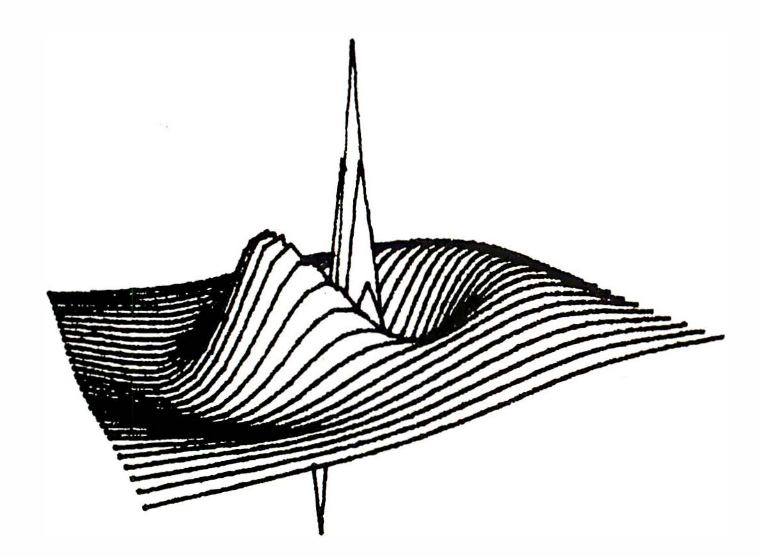


Figure 9: A plot made without crosshatching.

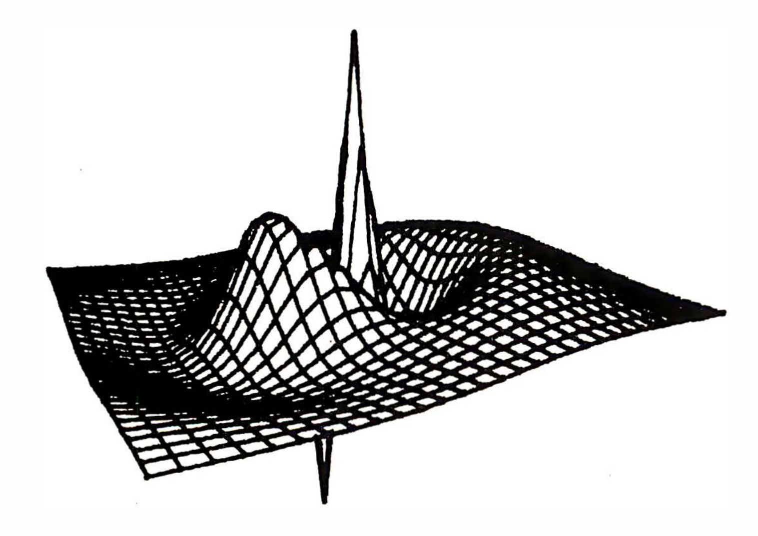


Figure 10: The same function as figure 9, but with crosshatching.

(X9,Y9), respectively. Then GOSUB 5500 (the fill-in points for the matrix subroutine) will fill in all the Y values for each X value along this line segment. Do the same thing for the right side, or the last point in each line.

The subroutine in listing 3 is accessed at the beginning and end of each line for the left side and the right side, respectively. X3 and X4 are initially set equal to −1 at the beginning of the program. This tells the routine that it is the first point in the graph and thus a line cannot be drawn between it and the previous point, which does not exist. After the first line is drawn, the previous points become (X4,Y4) and (X3,Y3) for the left and right sides respectively. S9 is the slope of the line needed in the fill-in routine.

Crosshatching is a method of drawing graphs with sets of orthogonal lines. For many graphs, this enhances the overall appearance and definition. The crosshatch program draws two separate graphs, one for the horizontal direction, and the other for the vertical. When the graph in the horizontal direction is completed, all initial conditions used in the hidden line subroutine must be reset. This includes reinitializing by placing the 0s and 800s into the 1024 by 2 matrix as described earlier.

One must also change the FOR NEXT loops for the X and Y axis: instead of keeping the Y value constant while stepping along in the X direction for a complete line, we hold the X value constant while stepping along in the Y direction.

A more efficient method consists of assuming the X to be the Y and the Y to be the X the second time around. An example is shown in listing 4. Matrix A contains the X,Y and Z values for use in rotation. Matrix Q is the final three-dimensional rotation matrix calculated elsewhere in the program. In the B loop, B = 0 is for the horizontal direction, B = 1 for the vertical direction. Notice the values assigned to matrix A when B changes from 0 to 1. Function FNP is the perspective function defined in the beginning of the program. GOSUB 5000 is for the hidden line subroutine. The function is for the graph shown in figure 7. Figures 9 and 10 show the effects of crosshatching.

In certain graphs, such as figure 11, lines must go behind very narrow regions. Here in the upper portion of the spikes we encounter difficulties. Using the method described so far for hidden lines, we solve for a new point and test to see whether that point is behind something. We can now determine if it should be hidden. Let us see what happens when we

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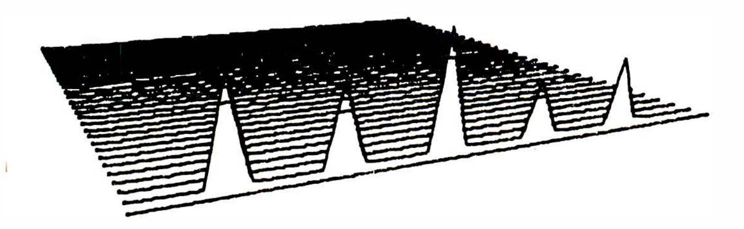


Figure 11: Problems can occur when lines go behind very narrow regions, but the line's endpoints are both visible.

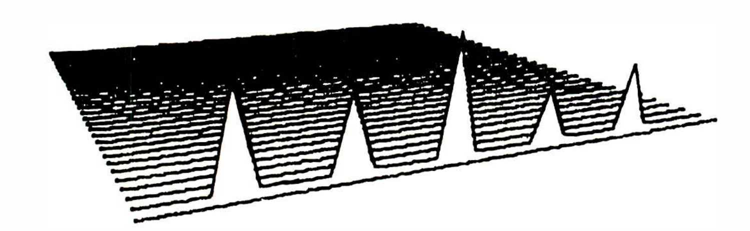


Figure 12: Solution to the problem illustrated in figure 11. The routine checks additional points along the line segment and makes changes accordingly.

```
100   00=1
110   U4=0,F=U5=1
120   L9=75
130   FILES *,*
140   ASSIGN "BLANK",2,T2
150   DIM A[1,3],C[1,3]
160   DIM Q[3,3],B[1024,2]
165   REM PERSPECTIVE FUNCTION
170   DEF FNP(F)=D7*F/(D7-C[1,3])
180   REM E=STEP VALUE AND K= # STEPS
190   E=10,K=20
200   I=-E,I2=E
210   REM D7=DISTANCE FROM (0,0,0) FOR PERSPECTIVE
220   D7=30
230   REM X2,Y2,Z2 ARE DEG. TURN AROUND X,Y,&Z AXIS
240   X2=-75,Y2=0,Z2=30
250   W=3.1416/180
260   X2=W*X2
270   Y2=W*Y2
280   Z2=W*Z2
290   GOSUB 6000
300   X3=Y3=X4=Y4=-1
310   READ #2,1
320   MAT READ #2;B
325   REM Y AXIS LOOP
330   FOR T=-E TO E STEP E/K
340      IF T>-.05 AND T<.05 THEN T=0
345      REM X AXIS LOOP
350      FOR G=-E TO E STEP E/K
360         IF G>-.05 AND G<.05 THEN G=0
370         U9=G
380         R=SQR(G*G+T*T)
390         A[1,1]=G
400         A[1,2]=T
405         REM ACTUAL FUNCTION
410         A[1,3]=8/(R+1)*COS(R*1.2)
420         MAT C=A*Q
425         REM SCALING, PERSPECTIVE & OFFSET
426         REM GOSUB TO HIDDEN LINE ROUTINE
430         X=FNP(C[1,1]*300/E)+512
440         Y=FNP(C[1,2]*300/E)+400
450         GOSUB 5000
460      NEXT G
470   NEXT T
480   END
```

Listing 6: A BASIC program used to create the plot shown in figure 13. Two subroutines, at line numbers 8100 and 8200, are not included in this listing, but must be supplied by the user. These are a routine to draw an invisible vector to point (x,y) at line number 8100, and a routine to draw a visible vector to point (x,y). These correspond respectively to the movement of a plotter's pen without contact and with contact. The details of the routines depend on the display hardware used.

```
5035   L8=SQR((X-X9)^2+(Y-Y9)^2)
5040   IF L8>L9 THEN DO
5045      L2=X9,L5=X,L6=Y,S6=(Y-Y9)/(X-X9)
5050      L7=(X-X9)/(L8/L9),L4=Y9-S6*X9
5060      FOR X=L2 TO L5-L7 STEP L7
5065         Y=S6*X+L4
5070         GOSUB 5090
5075      NEXT X
5080      X=L5,Y=L6
5085   DOEND
```

Listing 5: A routine used to refine the hidden line algorithm so it can correctly handle line segments which are visible at each end but obscured in the middle (see figures 11 and 12).

approach and go behind the upper portion of one of the spikes in figure 11.

Suppose the new point is just to the left of one of the spikes. The hidden line routine sees that the point is visible and should therefore have a line drawn to it from the previous point. Suppose the next point is behind the spike: the hidden line routine will see this and draw a line to the intersection point on the left edge of the spike. All is well and the graph continues.

But suppose on the next pass (near the tip of the spike) that the next point is again just to the left of the spike. It should be visible, so we draw a line to that point from the previous point. If the next point is to the right of the spike, the hidden line routine sees that this point on the graph should be seen, and thus a line is drawn from the previous point (which is to the left of the spike) to the point on the right of the spike. A line is drawn across the spike. This problem is apparent in the figure.

The problem of lines going through narrow regions which are in front is caused by the fact that the hidden line routine checks only to see if a line should be hidden at the endpoints of each line. If both endpoints are outside of the spike, it does not know that it is crossing the spike and draws a line across the spike.

The only way to overcome this problem is to check at points between the two endpoints to see if they go behind any region. If so, draw the line accordingly to hide any portion of the line that goes behind the region.

Here is a method for solving this problem. At the beginning of the program, decide on a maximum length of segment you wish to draw. If you are using a length of 5, for example, and the length of a normal line from endpoint to endpoint is 60, the program would divide this line into 12 segments and use the hidden line routine as though these were 12 consecutive lines. One should choose the maximum length of line on the

Listing 6, continued:

```
4985  REM U1 Thru U9;S7-S8-S9;X1,Y1 Thru X9,Y9 **  } Variables used in the Hidden Line Routine
4987  REM U8=0 (Last In); U8=1 (Last out) ***********  }
4990  REM ***SET I=1ST X & I2=LAST X  ***********  } Variables to set at beginning of Program
4992  REM ***U4=0,F=U5=1 * X4=Y4=X3=Y3=-1  ****  }
4995  REM ***** Let U9 = Value of X step  ***********
4997  REM SET L9= MAXIMUM LENGTH OF LINE ****
5000  IF X>1023 OR X<1 THEN U4=1
5005  IF X>1023 OR X<1 THEN RETURN
5010  IF U9=I AND Y<B[X,1] and Y >B[X,2] THEN 5140
5015  IF U9=I OR U4 THEN GOSUB 5600
5020  IF U9=I2 THEN GOSUB 5700
5025  U3=0
5030  IF U9=I OR U4 THEN 5155
5033  IF X-X9=0 THEN 5125
5034  REM STEPS 5035-5085 DIVIDE LINES INTO LINES OF LENGTH L9
5035  L8=SQR((X-X9)^2+(Y-Y9)^2)
5040  IF L8>L9 THEN DO
5045      L2=X9,L5=X,L6=Y,S6=(Y-Y9)/(X-X9)
5050      L7=(X-X9)/(L8/L9),L4=Y9-S6*X9
5060      FOR X=L2 TO L5-L7 STEP L7
5065          Y=S6*X+L4
5070          GOSUB 5090
5075      NEXT X
5080      X=L5,Y=L6
5085  DOEND
5090  IF X-X9=0 THEN 5145
5099  U3=0
5100  S9=(Y-Y9)/(X-X9)
5105  IF U8=0 THEN 5400
5110  IF Y<B[X,1] AND Y>B[X,2] THEN 5205
5115  U8=1
5120  IF U9=I THEN 5155
5125  GOSUB 8200
5130  GOSUB 5500
5135  GOTO 5145
5140  U8=0
5145  X9=X,Y9=Y
5150  RETURN
5151  REM RETURN TO MAIN PROGRAM
5155  X9=X,Y9=Y
5160  GOSUB 8100
5165  GOSUB 8200
5170  U4=0
5175  U8=1
5180  RETURN
5181  REM RETURN TO MAIN PROGRAM
5200  REM *** FIND INTERSECT ***
5205  S7=X-X9,U2=0,X1=X9,U1=1
5210  UNTIL U1>128 DO
5215      U1=U1*2
5220      IF U2 THEN 5235
5225      X1=X1+S7/U1
5230      GOTO 5240
5235      X1=X1-S7/U1
5240      Y7=S9*(X1-X9)+Y9
5245      IF U3 THEN 5456
5250      IF Y9>B[X9,2] THEN 5270
5255      IF Y7>B[X1,2] THEN U2=1
5260      IF Y7<B[X1,2] THEN U2=0
5265      GOTO 5280
5270      IF Y7<B[X1,1] THEN U2=1
5275      IF Y7>B[X1,1] THEN U2=0
5280  DOEND
5285  X5=X,Y5=Y
5290  X=X1,Y=Y7
5295  IF U3 THEN GOTO 5425
5300  U8=0
5305  GOSUB 8200
5310  GOSUB 5500
5315  X9=X5,Y9=Y5
5320  RETURN
5321  REM RETURN TO MAIN PROGRAM
5400  REM ***TEST U8=0***
5401  REM U8=0 IF LAST POINT WAS HIDDEN
5405  IF Y>B[X,2] AND Y<B[X,1] THEN 5145
5410  U8=1,U3=1
5415  X8=X,Y8=Y
5420  GOTO 5205
5425  GOSUB 8100
5430  GOSUB 8200
5435  X=X8,Y=Y8,U8=1
5450  GOTO 5125
5454  REM PART OF THE INTERSECTION ROUTINE
5455  REM ** FOR U3=1 :COMING OUT ***
5456  IF Y>B[X,1] THEN 5460
5457  IF Y7<B[X1,2] THEN U2=1
5458  IF Y7>B[X1,2] THEN U2=0
5459  GOTO 5280
5460  IF Y7>B[X1,1] THEN U2=1
5465  IF Y7<B[X1,1] THEN U2=0
5470  GOTO 5280
5500  REM ***** FILL IN POINTS *****
5505  U6=SGN(X-X9)
5510  IF U6=0 THEN 5535
5515  FOR U7=X9 TO X STEP U6
5520      S8=Y9+S9*(U7-X9),B[U7,2]=B[U7,2] MIN S8,B[U7,1]=B[U7,1] MAX S8
5530  NEXT U7
5535  RETURN
5600  REM ** FILL IN LEFT SIDE **
5610  IF X4#-1 THEN GOTO 5640
5620  X4=X,Y4=Y
5630  RETURN
5640  X8=X9,Y8=Y9
5650  X9=X4,Y9=Y4
5660  S9=(Y-Y9)/(X-X9)
5670  GOSUB 5500
5680  X9=X8,Y9=Y8
5690  GOTO 5620
5700  REM ** FILL IN RIGHT SIDE **
5710  IF X3#-1 THEN 5740
5720  X3=X,Y3=Y
5730  RETURN
5740  X8=X9,Y8=Y9
5750  X9=X3,Y9=Y3
5760  S9=(Y-Y9)/(X-X9)
5770  GOSUB 5500
5780  X9=X8,Y9=Y8
5790  GOTO 5720
6000  REM MAT ROTATE
6001  REM 6010-6110 MAKES MATRIX Q THE
6002  REM FINAL ROTATIONAL MATRIX
6010  MAT Q=ZER
6020  Q[1,1]=COS(Z2)*COS(Y2)
6030  Q[2,1]=-1*SIN(Z2)*COS(Y2)
6040  Q[3,1]=-1*SIN(Y2)
6050  Q[1,2]=COS(Z2)*(-1)*SIN(X2)*SIN(Y2)+SIN(Z2)*COS(X2)
6060  Q[2,2]=SIN(Z2)*SIN(X2)*SIN(Y2)+COS(Z2)*COS(X2)
6070  Q[3,2]=-1*SIN(X2)*COS(Y2)
6080  Q[1,3]=COS(Z2)*COS(X2)*SIN(Y2)+SIN(Z2)*SIN(X2)
6090  Q[2,3]=-1*SIN(Z2)*COS(X2)*SIN(Y2)+COS(Z2)*SIN(X2)
6100  Q[3,3]=COS(X2)*COS(Y2)
6110  RETURN

8100  REM A ROUTINE TO DRAW AN INVISIBLE VECTOR TO (X,Y)
8101  REM OR TO PICK THE PEN UP TO LOCATION (X,Y) (NOT INCLUDED)
8200  A ROUTINE TO DRAW A VISIBLE VECTOR TO (X,Y) (NOT INCLUDED)
9999  END
```

Figure 13: A representative plot with the hidden line subroutine. The program to generate it is shown in listing 6.

basis of the screen resolution and the accuracy desired. For greatest accuracy, use 1 as the greatest length of a line. This would, however, take a very long time to compute and draw. A happy medium should be chosen depending on the graph being drawn. Figure 12 shows the results of using this method.

Listing 5 is the routine used in the hidden line routine to divide each line into lengths no longer than L9. X9 and Y9 are the coordinates for the previous point. L8 is the length of the line being tested. GOSUB 5090 sends the new coordinates into the remaining portion of the hidden line routine. This routine may not be elegant, but it does work.

Listing 6 is the complete listing for the graph plotted in figure 13. I have given a complete program to help the programmer when any specific obstacles come up which are not explained in this article.

The program still contains a few "bugs" which crop up occasionally due to the simplicity of the algorithms used, so it is by no means the ultimate hidden line program. If any readers can write that ultimate hidden line routine, please let me know.■

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PLOT3D: A Function Plotting Program

Mike Stoddard
16681 Lynn St
Huntington Beach CA 92649

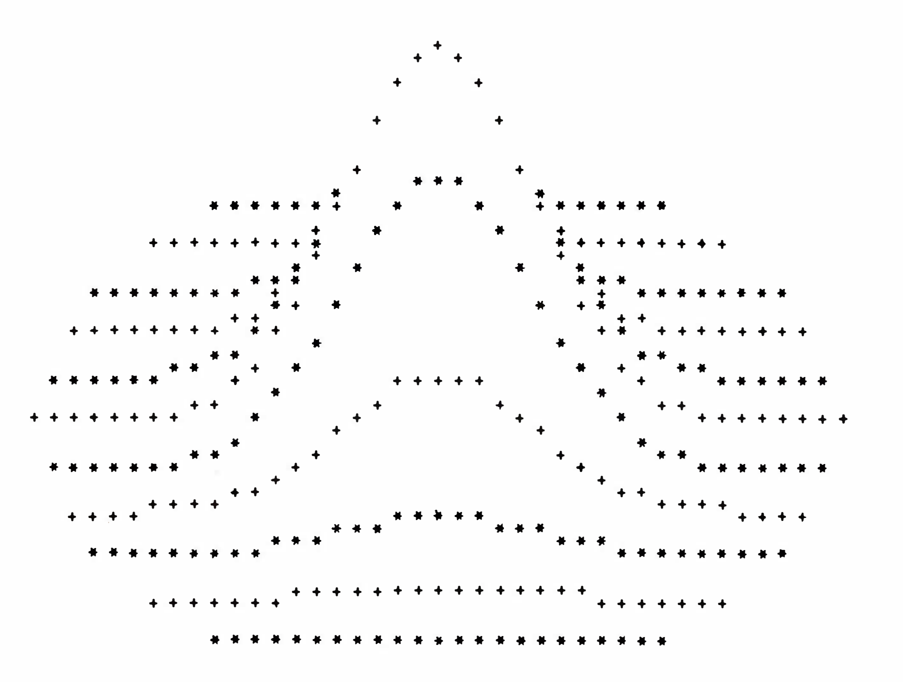


*Figure 1: Plot of Z = -30 * EXP(-f(x,y)^2 / 100)*
*(DEF FNA (Z) = -30*EXP(-Z*Z/100))*

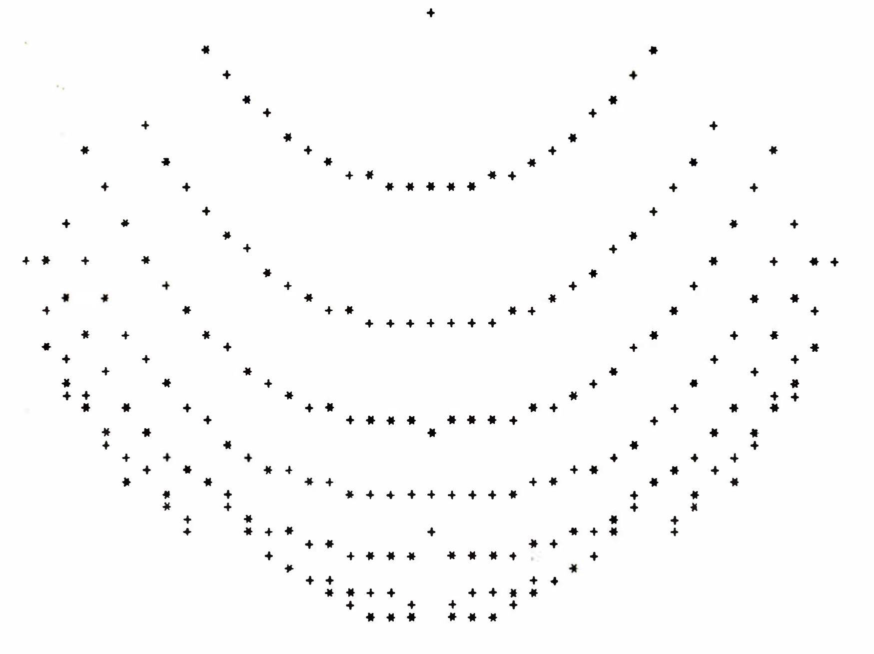


*Figure 2: Plot of Z = .001 * (f(x,y)^3 + f(x,y) - 25)*
(DEF FNA (Z) = .001(Z*Z*Z+Z-25))*

Most programmers have used FORTRAN or BASIC to generate a two-dimensional plot as part of their program. If they needed a three-dimensional plot, it was usually done on a pen plotter instead of printer or terminal output devices. Since most small systems lack a pen plotter, this program may be used to give a three-dimensional rendering of a normally two-dimensional function. By printing the third axis horizontally along the carriage of the terminal, the usual "hidden line" problem becomes trivial. In the sample program of listing 1, line 60 defines an exponential cosine function which normally plots as a decaying sinewave. Line 120 sets up the X axis values to be in the range -30 to +30. Line 160 calculates the Y axis values based on the expression $30^2 - X^2$, hence the X-Y axis sectional will be circular (remember the general equation of a circle is $X^2+Y^2=R^2$, where R will be the radius). The Z axis coordinate is then calculated in line 190 and the tilted 45 degrees to give a rotated view. Lines 200 through 290 pick the correct plotting symbol to use and then decide whether the point is visible or hidden. To correctly view the finished plot, remove it from the terminal, rotate it back 90 degrees, and then do a little "curve-fitting" by connecting the dots along the lines of corresponding symbols.

To change the plotted equation, redefine function A (called FNA in the program) in line 60. Figure 1 shows the plot of the equation given in the program. Figures 2, 3, and 4 show different functions and their corresponding plots. Note that all figures have been rotated left by 90 degrees from the way they are actually printed.■

```
 10 REM "PLOT3D" == FUNCTION PLOTTING PROGRAM
 20 REM WRITTEN BY MIKE STODDARD      03-03-77
 30 REM
 40 REM FIRST, DEFINE A NORMAL 2-DIMENSIONAL FUNCTION.
 50 REM IN THIS CASE, IT WILL BE A DECAYING COSINE
 60 DEF  FNA(Z)=30* EXP (-Z*Z/100)
 70 DIM A$(2),B$(1)
 80 REM DEFINE THE PLOTTING SYMBOLS
 90 LET A$="+*"
110 LET K=5
120 FOR X=-30 TO 30 STEP 1.5
130   LET L=0
140   LET P=1
150   REM CALCULATE X-Y PLANE PLOT LIMITS
160   LET Y1=K* INT ( SQR (900-X*X)/K)
170   FOR Y=Y1 TO -Y1 STEP -K
180     REM CALCULATE Z AXIS VALUES AND TILT 45 DEGREES
190     LET Z= INT (25+ FNA( SQR (X*X+Y*Y))-.707106*Y)
200     GOSUB 340
210     REM TEST FOR HIDDEN LINE
220     IF Z<L GOTO 300
230     LET L=Z
240     REM TEST FOR SAME PLOT LINE
250     IF P IF Z=Z1 GOSUB  340
260     PRINT         TAB (Z);B$;
270     REM SET HIDDEN/VISIBLE PLOT POINT
280     IF P LET Z1=Z
290     LET P=0
300   NEXT Y
310   PRINT         " "
320 NEXT X
330 GOTO  390
340 REM SWITCH THE SYMBOLS SO ALL POINTS ON
350 REM ONE LINE WILL BE THE SAME SYMBOL
360 LET B$=A$
370 LET A$=A$(2),B$
380 RETURN
390 END
```

Listing 1: The program "PLOT3D" used for three-dimensional projections into two-dimensional plots. The function defined at line 60 is plotted by the terminal printer using standard graphics of an ASCII character set.

*Figure 3: Plot of Z = 30 * (EXP(−f(x,y)² / 100) + SIN(f(x,y) / 5))*
(DEF FNA (Z) = 30(EXP(−Z*Z/100)+SIN(Z/5)))*

*Figure 4: Plot of Z = 30 * SIN(f(x,y) / 5)*
*(DEF FNA (Z) = 30*SIN(Z/5))*

GRAPH:

A System for Television Graphics

Part 1

John Webster
John Young
Audio Visual Services
University of New Brunswick
Keirstead Hall
Fredericton NB CANADA E3B 5A3

Our department of Audio Visual Services at the University of New Brunswick makes extensive use of small format videotape recording for instructional and research purposes. Tapes are recorded either in a studio situation or with portable recorders. Most programs are then edited, and require the addition of graphics ranging from simple titles or names superimposed over the picture to more complex charts and graphs that will be incorporated in the final production.

Anyone who watches television will have noticed that electronic character generators are becoming increasingly popular for providing titles, credits and other forms of alphanumeric character displays. Their advantages over the old system of creating the graphics on cards and pointing a camera at them are obvious. Electronic generators are quicker, require no special graphics training or materials, and are, incidentally, cheaper. Electronic titles can also be easily and quickly changed or updated. They also require no dedicated graphics camera and operator.

In examining commercial electronic titling equipment, we found two main disadvantages: Commercial units were quite expensive, and at the same time somewhat limited in their behavior.

We therefore decided to explore the "hobby" computer market and to design our own television graphics generator. The cost of our system turned out to be about half that of the cheapest commercial product then available, while giving increased flexibility for graphics handling. The computer system is also available for other uses when not being used for television graphics in our studio.

The hardware system we finally arrived at consists of an Altair 8800 with 17 K bytes of programmable memory, a Processor Technology VDM-1 with CUTS board, and a keyboard and cabinet modified from a surplus hotel reservation terminal. The program we developed to provide the necessary functions is the reason for this article.

The project was very much a learning experience, since we assembled both the hardware and software. With the exception of a hardware approach to providing a keyboard repeat function, this article is concerned primarily with the software, since it is more likely to be applicable to a greater number of varied systems.

Instead of simply publishing a commented assembly listing of the program, we have gone into considerable detail about the structure of each subroutine and about the workings of the VDM-1 on which the program is based. It is hoped that the program will be useful to many who are using a VDM-1 in any related way, and that the article will serve as a learning tool for anyone new to low level assembly language programming.

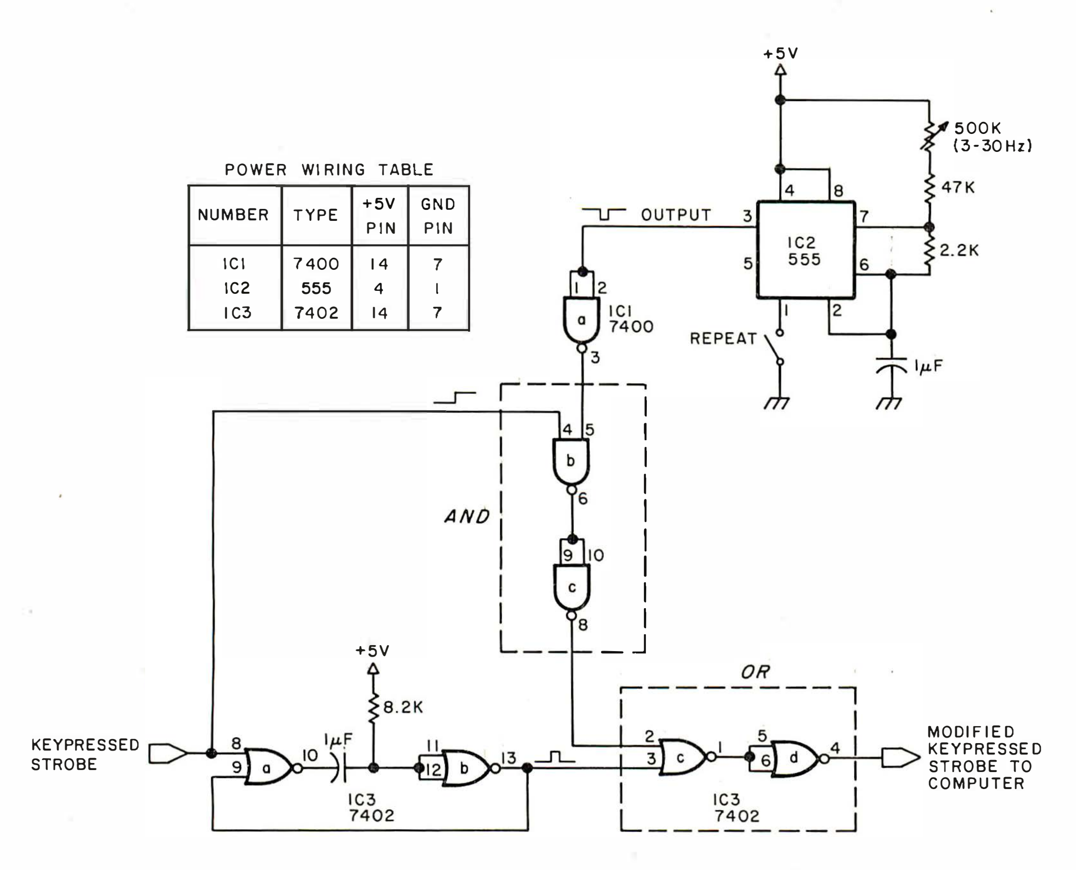
The Repeat Function

A repeat function is a facility to generate repeated inputs of a keyboard key's code when the key is held down for extended periods of time. Two approaches are offered to the problem of providing a repeat function, one in hardware and one in software. The hardware approach offers the advantage of a more easily variable speed, while the software approach requires no hardware changes and is executable on any keyboard.

When a computer keyboard key is pressed, two signals are generated. One is an

Authors' Note:

This project was a valuable learning experience for us. Attempting to explain a program step by step in English turns out to be a bit lengthy, but we hope that the final result is a package with real teaching and learning potential for anyone new to 8080 machine language programming or the VDM-1. It is exactly the kind of article we wish we had had access to a year ago when we first plugged in our VDM-1 and wondered what to do next.



POWER WIRING TABLE

NUMBER	TYPE	+5V PIN	GND PIN
IC1	7400	14	7
IC2	555	4	1
IC3	7402	14	7

Figure 1: Interface circuitry for GRAPH. An astable multivibrator (IC2) provides the pulse train for a hardware repeat function. The authors' keyboard produces a low to high transition strobe (STB) pulse when a key is pressed. This is used to trigger a monostable multivibrator to provide a single pulse keypressed (KP) signal to interface with the IO board used.

A logical AND function gates the astable multivibrator's output with STB to generate a repeat only when a valid character key is pressed. A logical OR routes either a repeat pulse train or a single KP signal to the computer's IO board.

Because the repeat key on the authors' keyboard is tied to ground, it is used to interrupt the ground connection (pin 1) of the 555 timer. This design seems to work satisfactorily. If a normal single pole single throw switch is available, a more proper design would be to interrupt the output (pin 3).

8 bit binary number corresponding to the character chosen. The other is a "keypressed" signal that tells the IO board a key has been pressed and it should read and input the eight bit number as valid data.

If a pulse train instead of a single pulse is presented on the keypressed line to the IO board, the computer will continuously input the 8 bit character word presented as a series of characters. A repeat function will occur as long as the pulse train is present. A potentiometer varying the frequency of the pulse train will produce a variable speed repeat.

The circuit in figure 1 uses a 555 timer (IC2) to generate the repeat pulse train and apply it to the keypressed line. Notice that it is important to gate the pulse train with the original keypressed STROBE DC level from the character generator line so that the oscillator will operate only when a character key is pressed. Otherwise, invalid data will be input if the repeat key is pressed before a character key.

Another handy circuit is contained in figure 1 (lower lefthand corner). Most keyboards presently available provide a low to high strobe transition to indicate a key is pressed. Many IO boards, however, require a single pulse to latch the valid data. This portion of the circuit in figure 1 converts a DC strobe level to a single pulse output.

A software approach to achieving a repeat function is discussed in the Program Design section.

Using the VDM-1

The heart of the graphics generator is, of course, the VDM-1. Like several other television boards available, it contains 1 K bytes of programmable memory which hold the 16 lines of 64 characters per line that appear on the screen. Thus, manipulating

FIRST INVALID ADDRESS
(TOP OF SCREEN)

CBFF

LINE NUMBER	FIRST OF LINE ADDRESSES	END OF LINE ADDRESSES
1	CC00	CC3F
2	CC40	CC7F
3	CC80	CCBF
4	CCC0	CCFF
5	CD00	CD3F
6	CD40	CD7F
7	CD80	CDBF
8	CDC0	CDFF
9	CE00	CE3F
10	CE40	CE7F
11	CE80	CEBF
12	CEC0	CEFF
13	CF00	CF3F
14	CF40	CF7F
15	CF80	CFBF
16	CFC0	CFFF

D000

FIRST INVALID ADDRESS
(BOTTOM OF SCREEN)

Figure 2: Visualization of line starting and ending addresses in GRAPH. This type of information is helpful in understanding the subroutines that check for valid screen addresses. The Processor Technology VDM-1 displays 16 lines of 64 characters per line which reside in 1 K bytes of programmable memory.

graphics becomes merely a question of manipulating digital information in a 1 K byte workspace.

Data from any register can be moved to the screen with a MOV M, X (whose X is any register) instruction. The position on the screen is determined by the 16 digit number in the H, L register pair, which in this case would be between hexadecimal CC00 (first screen position) and CFFF (last screen position). Allocations of the starting and ending line addresses, as well as the first invalid address on either side of the screen, are shown in figure 2.

The VDM-1 is designed to display a cursor if bit 8 is high, regardless of the status of the other 7 bits. If cursors appeared at all screen positions, the screen would appear white instead of black. Lines or blocks of cursors may be used to draw simple figures.

One shortcoming of the VDM-1 display is that a full cursor is the smallest contiguous unit available. The available graphic resolution is therefore a matrix of only 64 by 16 blocks.

The VDM-1 also contains a scrolling feature which allows vertical displacement of screen contents. It was decided not to use this feature in our program for reasons that will be explained later.

The output of the VDM-1 is a video signal containing both horizontal and vertical synchronizing pulses which permit display of the graphic information on any television monitor. It should be noted that the horizontal and vertical drive pulses are slightly nonstandard; and, although they will be accepted by any television monitor, they may not synchronize easily with more sophisticated video recording or signal processing equipment. The Digital Group has announced a 1 K byte video display control board that can be driven by external sync pulses. Since GRAPH is written specifically for the VDM-1, some changes in approach (for example, cursor handling) may be necessary when using video display boards from other manufacturers.

In order to make the VDM-1 do anything at all, you need a driver program. For example, a simple program could be written to take a character and type it into the screen starting at the upper left hand corner (hexadecimal address CC00). To do this it would be necessary to:

Load H, L with hexadecimal CC00	first screen position
→ Check for status	has a key been pressed?
Read value of key pressed and store in accumulator (A)	
Move A → M	move character to screen
Increment H, L	move to next screen position
Loop to status check	get ready for next character

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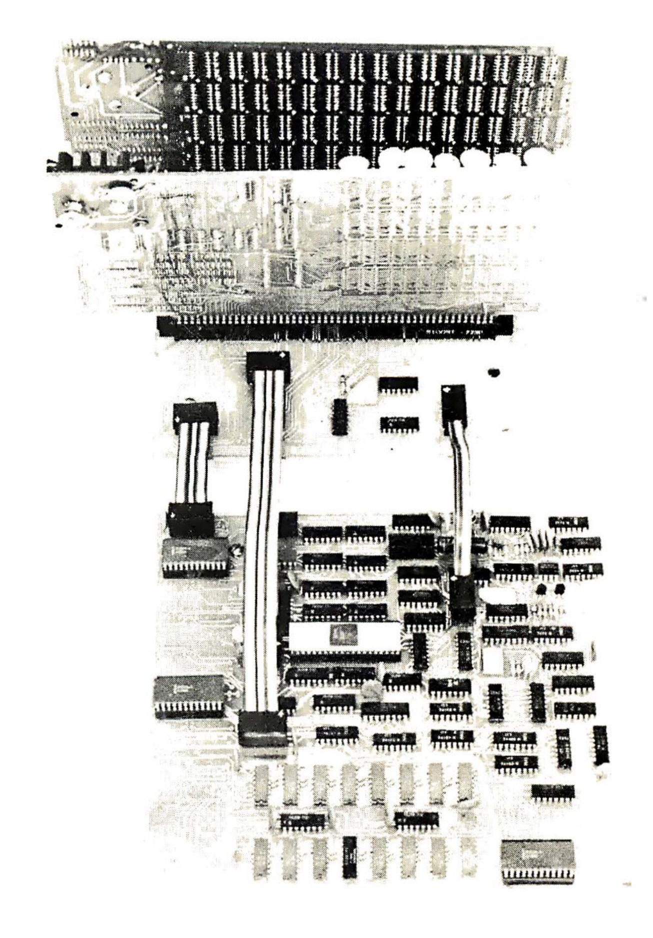
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START
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CLEAR
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CCOO → H, L
CURSOR
REPEAT STATUS WORD SET ?
YES
GO THROUGH I CYCLE OF DECREMENT TIMING LOOP
NO
HAS ANOTHER KEY BEEN PRESSED ?
YES
RESET REPEAT STATUS WORD
NO
STATIN HAS KEY BEEN PRESSED ?
NO
E
YES
DATIN INPUT DATA
OR DATA WITH CURSOR. WRITE STATUS WORD
CONTROL CHARACTER CHECK ?
YES
NO
PRINT CHARACTER ON SCREEN
IN VERTICAL WRITE MODE ?
YES
LINEFEED (AT LFP)
NO
INX(H)
CHECK FOR END OF SCREEN ?
NO
YES
A
B
C
D

CTRL/V	LINEFEED	
CTRL/T	LINE RETRACT	
CTRL/F	BACKSPACE	
CTRL/G	FORWARD SPACE	
CTRL/J	CRLF	
DEL	DELETE	BACKSPACE (AT BSP)
CTRL/U	PAGE UP	LINE RETRACT (AT LRP)
CTRL/M	PAGE DOWN	LINEFEED (AT LFP)
CTRL/H	PAGE LEFT	BACKSPACE (AT BSP)
CTRL/K	PAGE RIGHT	FORWARD SPACE (AT FSP)
CTRL/P I, 2, 3, 4, 5, 6	PAGE RECALL	PAGE STORE (AT MOV I)
CTRL/S	PAGE STORE	
CTRL/R	REPEAT	
CTRL/Q	VERTICAL WRITE	
CTRL/A	CURSOR ON/OFF	
CTRL/Z	CURSOR WRITE/ DON'T WRITE	
CTRL/W I, 2,3, 4,5, 6.	NEXT STORE ADDRESS SET	
CTRL/W CLEAR	SYSTEM CLEAR CLEAR SCREEN INIT CURSOR INIT STATUS WORDS	
CLEAR	CLEAR SCREEN INIT CURSOR	
CTRL/X	HOME CURSOR	
ESC	ESCAPE	JUMPS TO ADDRESS LOCATED AT HEXIDECIMAL 346 AND 347

D
E
A
B
C
D

Figure 3: A global system chart for GRAPH.



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Type Characters Onto Screen			Happens automatically for all noncontrol characters.
Repeat	CTRL/R,X	012	Repeats character X until any key is pressed.
Move Cursor Up Down Right Left	CTRL/T CTRL/V CTRL/G CTRL/F	014 016 07 06	Cursor may be moved around screen in either "cursor write" or "transparent" mode.
Cursor Write/ Don't Write	CTRL/Z	01A	Cursor blocks may be used to draw lines or figures.
Cursor On/Off	CTRL/A	01	Leading cursor appears or disappears.
Clear Screen	Clear	01C	Clears screen and initializes cursor to upper lefthand corner.
Home Cursor	CTRL/X	018	Cursor is initialized to upper lefthand corner without clearing screen.
CRLF	LINEFEED or (CTRL/J)	0A	Generates a carriage return and linefeed sending leading cursor to lefthand end of next line.
Move Screen Up Down Right Left	CTRL/U CTRL/M CTRL/K CTRL/H	015 0D 0B 08	Entire contents of screen may be shifted up, down, right or left.
Vertical	CTRL/Q	011	Allows character entry in vertical columns.
Store	CTRL/S	013	Entire contents or screen may be stored in one of six rotating locations.
Recall	CTRL/P 1, 2, 3 4, 5, 6	010	Contents of any previously stored screen may be recalled.
Choose Storage Location	CTRL/W 1, 2, 3 4, 5, 6	017	Screen storage status control word is set to chosen value for next STORE.
System Initialize	CTRL/W CLEAR	017 01C	All systems parameters and storage registers are initialized, screen is cleared and cursor returned to upper lefthand corner.
Escape	ESC	01B	Exit from GRAPH and return to system monitor.
Delete	DEL	07F	Writes blank into present position and moves leading cursor back one space.

Table 1: Program functions in GRAPH and their specific control characters.

If you implement such a program, you will immediately see that it is not very flexible, and the need for refinements will become apparent. What about a cursor? What if you want to start typing somewhere else, make changes, draw lines, etc?

We asked ourselves the same questions and more. The result was GRAPH, a multifunction video display memory handler. The following sections will detail the design and implementation of GRAPH step by step.

Program Function and Use

The GRAPH program is designed to do practically everything we ever wanted to do with the VDM-1, to be as universally applicable and self-contained as possible, and to reside in the lowest 1 K byte of memory. (The store and recall functions require additional memory space; more about this next month in part 2.)

The program consists of a driver which waits for keyboard input and then checks for special control characters. If a specific control character is typed, one of a series of subroutines or special operations is entered. If the entered character is not a special control character, the typed information is displayed on the screen. Table 1 lists the program functions and their specific control characters.

GRAPH is designed so that all screen operations "wrap around" and therefore stay within the 1 K byte screen boundaries. For example, a leading cursor in the last screen position will appear in the upper lefthand corner (first screen position) when

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the next character is entered. Similarly, information moved off the top of the screen with a MOVE UP command will appear at the bottom of the screen. In this way, no information is lost and adjacent memory is not affected.

GRAPH may be entered either by a jump or a call. If a jump is used, hexadecimal memory locations 346 and 347 should be loaded with the desired address for a jump back to a system monitor program (eg: to return to ALS-8, 346 is set equal to hexadecimal 60, and location 347 is set equal to hexadecimal E0). If GRAPH is entered by a CALL instruction, hexadecimal memory location 345 should be loaded with an unconditional return, C9. In this case 346 and 347 are not used.

Program Design

To aid in understanding the operation of the program, it has been divided into three main sections: the Driver section, the Control Checks section and a section of Special Operations. Special operations are called into use by certain designated control characters.

Although most of these operations are distinct subroutines, several, such as Cursor (on/off) and Vertical Write, consist of only a few instructions in the Control Check section that modify the operation of the Driver section by changing certain status words in memory. Others, such as Home Cursor and System Clear are merely jumps to subroutines already existing inside the Driver section.

Descriptions of some of these routines are brief in certain cases because the operation of some subroutines is simple. Other techniques, however, such as using DAD instructions to subtract (as in the Move routines), will be examined in more detail.

To interface each subroutine with our program, certain standards have been adopted, as follows:

- In each subroutine, screen character positions are controlled by using the H and L register pair. Information is moved to the screen by using a MOV instruction to register M, which moves the data to the memory location specified by the address in H and L. Therefore, by changing the values of H and L, the memory location into which characters are to be input is changed.
- The only register "tied up" when leaving the Driver to execute a subroutine is register C, used to store the screen information previously located at the leading cursor position. The cursor which travels along to indicate the next entry position on the screen will be referred to as a "leading cursor."
- Since the cursor is a movable item, the first step upon entering most subroutines is "MOV M, C," which moves the information stored in C back to the screen and makes the leading cursor disappear. This then frees register C for use in the subroutine.

Driver Section

The heart of any multifunction program is the Driver, which has a number of functions:

- Initialization: Upon entering the program at its starting location, the first thing encountered is a jump to an Initialize subroutine. This simply involves setting the memory status words or locations to their initial values. This is accomplished by loading D and E with the hexadecimal value 03F5 and loading the accumulator with 00. Then a STAX operation is executed, which stores the accumulator at the location specified by D and E. The latter are incremented, and the STAX operation is again performed. This is repeated five times. The accumulator is then loaded with hexadecimal CC, the STAX operation is performed (location 3FA), and D and E are incremented. The accumulator is then loaded with hexadecimal 80 and the STAX operation performed (location 3FB). By this store and increment method, hexadecimal

Hexadecimal Location	Purpose	Hexadecimal Initialized Value
3FF 3FE	Save H and L for Screen Moves	Don't care
3FD 3FC	Save Stack Pointer	Don't care
3FB	Cursor On/Off	On = 80
3FA 3F9	Save H and L for Page Store and Recall	3FA = CC, 3F9 = 00
3F8	Page Store Status	Page 1 = 00
3F7	Vertical Write/ Not Vertical Write	Not Vertical Write = 00
3F6	Cursor Write/ Don't Write	Don't Write = 00
3F5	Repeat/ Not Repeat	Not Repeat = 00

Table 2: A table of values used by the initialization subroutine to set the memory status words or locations to their initial values.

locations 3F5 to 3F9 are initialized to zero, location 3FA to hexadecimal CC and location 3FB to hexadecimal 80. The initial contents of locations 3FC, 3FD, 3FE and 3FF are unimportant.

- Clear: The Clear subroutine writes blanks (hexadecimal A0) into every screen location and initializes the status of the video display module.

  The status of the module is initialized to display all 16 lines in a nonscrolled format by writing 00 into the VDM-1's status port (hexadecimal C8).

  The screen is cleared by initializing the H and L registers to hexadecimal CC00 (upper lefthand corner), loading that position with a blank, incrementing and loading a blank, and so on, until the screen is filled.
- Home: The operation then jumps to the HOME section of the Driver where H and L are again set to hexadecimal CC00 and the program proceeds to the CURSOR section.
- Cursor: CURSOR, by checking hexadecimal memory location 3FB, either prints a cursor and character, or just the character in this initial position (hexadecimal CC00).

CURSOR is responsible for printing the leading cursor everytime it appears on the screen. Hence, any subroutine which modifies H and L to change the "next character to be entered" location (such as Linefeed, Backspace, etc) must immediately jump to the CURSOR subroutine to decide whether or not to print a leading cursor in the new screen position.

During its operation, CURSOR first moves the contents of the screen location addressed by H and L to register C for safekeeping. It then loads the accumulator with the contents of memory location 3FB, which is either hexadecimal 00 or hexadecimal 80.

By ADDing the character in C to the accumulator, the accumulator is modified so that when it is displayed either just the character appears, or the character appears in a cursor block. For example, if the contents of memory location 3FB is hexadecimal 00, then moving this value to the accumulator and adding the character in C to the accumulator will leave just the character in the accumulator.

But if 3BF contains hexadecimal 80, then a white cursor will appear (on a black background), or a black or inverted cursor will appear (on a white background).

At this point, the status word at hexadecimal location 3F5 is checked to see if the program is in the Repeat mode. If 3F5 contains hexadecimal 00, then operation passes to the keyboard status check called STATIN. Here the operation loops until STATIN indicates that a key has been pressed. At this point the program inputs the data at DATIN and moves it to register B for safekeeping.

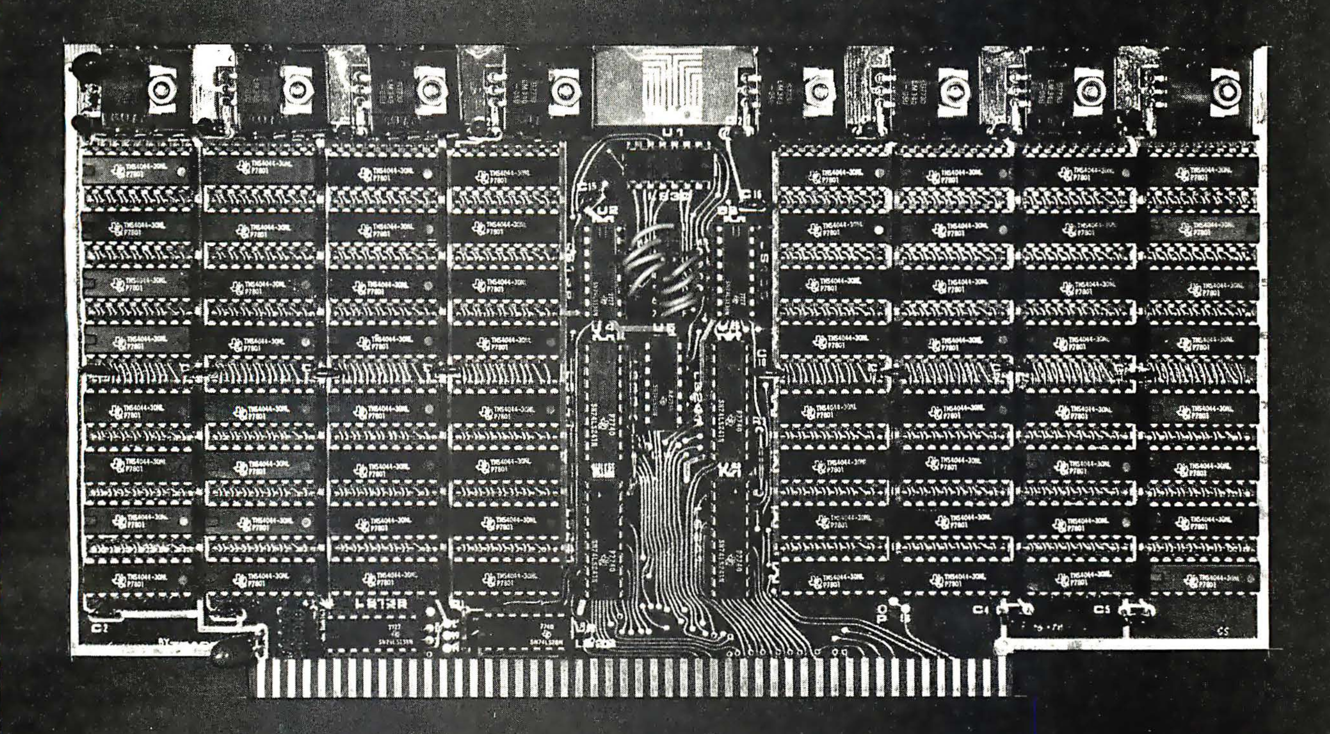
If location 3F5 contains hexadecimal 80, a jump is made to a timing delay loop. In this delay loop, D and E are loaded with hexadecimal 10FF and decremented until they reach zero. This provides a programmable delay between characters in the Repeat mode. Next, a keyboard status check is made by logically ANDing the keyboard word (IN 00) with hexadecimal 40. If the result is zero (meaning no key has been pressed since the character to be repeated was entered), then program operation jumps to DATIN, which inputs the unchanged data in IO port 01 to the accumulator. If the input data is a character to be printed, it is displayed on the screen and operation eventually returns through CURSOR to check the Repeat mode status again. As long as no other keyboard key is pressed, the program will continue to cycle through the delay timing loop, repeatedly displaying the entered character on the screen.

Those subroutines which jump back to the Driver at or above CURSOR may also use the Repeat function (see figure 3). If, for example, CTRL/R and then CTRL/V (Page Up) are entered, the display will continually roll upward until another character is entered to cancel the repeat function. When the character after CTRL/R is entered, an IN 01 is executed to reset the keyboard status, although the input data is not used in any way. The Repeat status word at location 3F5 is then reset to zero and operation jumps to STATIN.

Since the repeat delay is controlled by the value in D and E, varying this value affects repeat speed. New values may be entered at hexadecimal memory locations 282 and 283 to produce different speeds. Using a value of hexadecimal 0000 will result in the slowest speed (about 2 to 3 Hz). Hexadecimal 10FF produces a convenient speed of about 30 characters per second.

Following DATIN, the program next enters the Cursor write/don't write section, which loads the accumulator with the contents of hexadecimal address 3F6 (either hexadecimal 00 or hexadecimal 80) and logically ORs it with B. This new value (either just the character, or the character plus bit 8) is moved back into B as the valid desired data.

This in effect adds a cursor bit (bit 8) to the character input if Cursor write is desired,



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or leaves the character as is if no cursor is desired. Hexadecimal memory location 3F6 is loaded by the Cursor write/don't write subroutine (Control/Z) as hexadecimal 00 or hexadecimal 80 alternately. Thus, if the letter X is typed while location 3F6 contains hexadecimal 80, then X is printed on the screen enclosed in a cursor.

This section is analogous to a toggle switch controlling the state of bit 8, which might be an alternate hardware approach.

Next, the Driver jumps to the control check section to determine which subroutine (if any) has been selected. If a subroutine has been selected, the data in B is no longer important (since we don't want to print control characters on the screen), and B is free to be used in any subroutine.

Control Character Check

Although the Control Character Check section is part of the driver, it is physically separated from the driver in the assembly listing to facilitate expansion. The Control Character Check detects the presence of the various assigned control characters and routes the program operation to the respective subroutines or operations. Since the majority of the Control Character Checks consist simply of *compare immediate* and *jump if not zero* statements, only two internal routines, Page Recall and Control W, will be examined in detail.

Page Recall Control Check

Once the Control Character Check recognizes the code for Page Recall, it does a keyboard status check, waiting for the next character to be pressed. The character is then entered, and the cursor bit (bit 8) is peeled off or set to zero by logically ANDing with hexadecimal 7F. If the character entered is a number from 1 to 6, the compare statements in this nested subroutine transfer operation to the respective Page Recall location. If the character entered is not a number from 1 to 6, operation jumps back to STATIN in the Driver program.

Control W Check

Once a control W has been detected by the Control Character Check subroutine, the program waits for the operator to input another character. If the latter is a character from 1 to 6 or "clear," an operation is performed. If not, the program jumps back to STATIN in the Driver.

If 1 is pressed, hexadecimal memory location 3F8 (the page store select location) is loaded with the correct value (hexadecimal 00) so that the next Page Store will be stored in page 1. The same holds true for numbers 2 thru 6. Operation then jumps back to STATIN. However, if Clear is pressed, operation jumps to the Initialize and Clear sections of the Driver where *all* the memory status words are reset to their initial values and the screen is cleared. This operation is referred to as System Clear in the Control System Chart (see figure 3). At the end of any subroutine, the operation jumps back to the Driver program.

If no subroutine has been selected, the contents of B (the previously input data) are moved to the screen. The program first checks hexadecimal location 3F7 to see if it is in the Vertical Write mode, and then decides whether to increment to the next screen location (required in a normal character entering mode) or to go into the Vertical Write mode. In this last case no increment is produced, but a Linefeed is executed (the Vertical Write mode enables the user to enter the next character immediately below the previous one). This allows a vertical line of characters to be drawn downward. If the value of hexadecimal memory location 3F7 is zero, the program increments H and L normally. If it is anything other than zero, the Vertical Write mode is entered. The data in location 3F7 is controlled by the Vertical Write subroutine (CTRL/Q) which alternately loads it with hexadecimal 00 or hexadecimal 80.

Finally, the driver checks to see if it has reached the end of the screen (in Vertical Write mode, Linefeed takes care of this), and if so a jump is made to a location in the initializing section (HOME), thereby setting H and L back to their upper lefthand value. If the end of screen has not been reached, operation simply jumps back to the CURSOR section, which operates as explained above. The program is now ready for a new character.

Special Operations

There are 21 special operations which GRAPH performs. They will be examined in the following order:

1. Linefeed
2. Line Retract
3. Backspace
4. Forward Space
5. Carriage Return & Linefeed (CRLF)
6. Delete
7. Page Up
8. Page Down
9. Page Left
10. Page Right
11. Page Store
12. Page Recall
13. Repeat

14. Vertical Write
15. Cursor On/Off
16. Cursor Write/Don't Write
17. Next Store
18. System Clear
19. Clear Screen and Initialize Cursor
20. Home Cursor
21. Escape From GRAPH

Line Feed

This subroutine can be entered by pressing Control/V while the cursor write mode is either on or off. This simply means that Linefeed will be accessed with either hexadecimal 56 or hexadecimal D6 (the latter being a hexadecimal 56 with the cursor bit set equal to 1).

Note that this double control check is necessary only in the first four subroutines (Linefeed, Line Retract, Forward Space, Backspace), since these are the only routines used to draw cursors on the screen in addition to performing their own specific functions.

Before checking for the next control character after Backspace, therefore, the cursor bit is masked off by ANDing it with hexadecimal 7F, so that only single control checks are necessary for all further operations.

If Linefeed is accessed with the cursor bit set (LFC), register C is loaded with hexadecimal A0, a blank cursor. This value is moved to M (putting a blank cursor on the screen). Thus, in this mode, every Linefeed writes a blank cursor below the previous one. This can be used to draw a line downward on the screen.

If Linefeed is accessed in the Cursor "don't write" mode (LF), then the original information in C is transferred to M, leaving the screen in its pre-"leading cursor" state and freeing C for subsequent use if needed.

To accomplish its job, Linefeed loads registers D and E with hexadecimal 40 (decimal 64) and then adds this to H and L. This means that the next position to be entered on the screen will be 64 characters after the last one, exactly one line down (since lines are 64 characters long).

The subroutine then checks to see if this new value from H and L is valid; that is, if it is still on the screen. If it is a valid screen location, operation jumps back to CURSOR in the Driver. If not, it will be necessary to "wrap around" and move to the top of the same vertical row. In this case register H is loaded with hexadecimal CC. Since the position across a line is controlled by the value in register L, keeping the same value in L and setting H to hexadecimal CC produces a linefeed from the bottom of the screen to the top.

For example, with the cursor at the lowest lefthand screen position (refer to figure 2), H and L are hexadecimal CFC0 (H = hexadecimal CF, L = hexadecimal C0).

If a Linefeed is pressed at this point, H and L will be modified to hexadecimal D000, and the program will detect that this value is off the screen. Then, instead of jumping back to CURSOR, the program loads H with hexadecimal CC and leaves L at hexadecimal 00. Thus the next screen position is hexadecimal C000, which is the highest lefthand screen position. In this manner, a linefeed from any position on the bottom line moves the cursor to the corresponding position on the top line. The operation then jumps back to CURSOR in the Driver.

Line Retract

Whenever Line Retract is executed, the leading cursor position is moved up one line. Like Linefeed, it can be entered by a Control/T in either the Cursor "write" (LRC) or "don't write" (LR) mode. By using Line Retract while in the cursor "write" mode you can draw lines of cursors upward on the screen. Line Retract operates the same as Linefeed except that it adds FFC0 to H and L in order to move up one line, instead of adding hexadecimal 40, as in the case of Linefeed.

Since the 64 K byte memory wraps around from its last position (hexadecimal FFFF) to its first position (hexadecimal 0000), adding hexadecimal FFFF to any value of H and L will bring you around through memory and up to the memory location immediately preceding that value. Thus, adding hexadecimal FFC0 to a value of H and L will bring you to hexadecimal 40 (decimal 64) before that value. This has the effect of subtracting hexadecimal 40 from the current cursor position, hence backing up one line. The Line Retract subroutine also checks the new value of H and L to see if it is valid (on screen). If not, it loads register H with hexadecimal CF so that the new cursor position will wrap around from the top to the bottom of the screen, similar to Linefeed. Line Retract always finishes with a jump to CURSOR in the Driver.

Backspace

Backspace, like the preceding two subroutines, can be executed by a CTRL/F while the Cursor write mode is either on or off. Backspace writes cursors on the screen when the Cursor write mode is on by the

same method as Linefeed (ie: loading register C with A0H before moving C to M). The values of H and L are then incremented and a check is made to see if the new value is valid. If so, program operation jumps to the CURSOR section of the Driver. If not, the cursor has obviously been bumped off the upper lefthand corner of the screen. The backspace subroutine loads H and L with hexadecimal CFFF (the address for the lower righthand corner position), and then jumps to CURSOR. Thus, backspace wraps around from upper left to lower right.

Forward Space

Forward Space does the same as Backspace, but in the opposite direction. Cursors can be written using Forward Space if the Cursor write mode is on, as in the preceding three subroutines. In forward space, the cursor wraps around from the lower righthand corner to the upper lefthand corner. Forward space ends with a jump back to CURSOR.

The preceding four subroutines are all used either to move the leading cursor to the desired location of the next character, or to draw cursor lines up, down, back or forward. It should be noted that if the Cursor write mode is *off*, these subroutines move a transparent cursor over the screen. Whenever the cursor is moved in this mode, the contents of C (original value of that position) first replace the leading cursor, and the cursor is moved to the next location. In every case, the content of the new leading cursor location is stored in C before the cursor is displayed. Hence, all four of the preceding routines move "transparent" leading cursors around on the screen and do not destroy any screen information. In the Cursor write mode, any of the four routines will write cursors on the screen.

Carriage Return and Linefeed

Basic to understanding the operation of CRLF is the knowledge of the contents of the H and L register pair for various key screen positions (see figure 1).

Since there are hexadecimal 40 (decimal 64) characters per line on the screen, four lines of characters can be addressed solely by the L register (an 8 bit register can store up to 100 hexadecimal or 256 decimal combinations). Thus, the H register changes only once every four lines. The starting addresses of all 16 lines may be seen in figure 1.

The CRLF subroutine includes a Linefeed so that, when executed, the leading cursor moves to the start of the next line.

To perform this, the subroutine checks the current address contained in H and L and compares it with all line starting addresses to determine which line it is on. Having determined this, it sets H and L to the starting address of the next line and then jumps back to the CURSOR section of the Driver.

As in most subroutines, CRLF moves the contents of C to the correct screen position, restores the screen to its pre-"leading cursor" condition, and then loads the accumulator (A) with the contents of register L. Following this, it compares A with hexadecimal 40 by means of a CPI instruction, which subtracts hexadecimal 40 from A and sets the flags, but doesn't alter the contents of A.

If L is greater than or equal to hexadecimal 40, the program jumps to a location where another check is performed to compare L with hexadecimal 80.

If L is greater than or equal to hexadecimal 80, it is similarly compared to hexadecimal C0.

If L is less than hexadecimal 40 in the first check, however, the program loads L with hexadecimal 40 and jumps to OUT. Here, this new value of H and L is checked to determine if it is a valid screen address. If so, operation jumps back to CURSOR. If it is not a valid screen address, the program jumps to HOME, initializing H and L to hexadecimal CC00. Similarly if L is found to be less than hexadecimal 80 or hexadecimal C0, it is loaded with hexadecimal 80 or hexadecimal C0 respectively, and operation jumps to OUT as outlined above.

If L is found to be greater than or equal to hexadecimal C0, H is incremented, L is loaded with hexadecimal 00, and operation passes to OUT. To summarize:

If hexadecimal 0 ≤ L < 40,	L gets loaded with hexadecimal 40
If hexadecimal 40 ≤ L < 80	L gets loaded with hexadecimal 80
If hexadecimal 80 ≤ L < C0	L gets loaded with hexadecimal C0
If hexadecimal C0 ≤ L	H gets incremented and L gets loaded with hexadecimal 00

Examples:

Initial Values H	L		Hexadecimal Values After Carriage Return H	L
CC	20	→	CC	40
CC	42	→	CC	80
CC	90	→	CC	C0
CC	D1	→	CD	00
CF	D1	→	CC	00

Delete

When the Delete subroutine is entered, it moves a blank to the present cursor position and jumps to a section of the Backspace subroutine. This has the effect of deleting the character located at the present leading cursor position and moving the cursor back one space for a subsequent delete, if desired.■

This completes the first part of the presentation of the GRAPH package. Several of the functions listed in table 1 and found in figure 3 will be described in detail in part 2's continuation of the documentation. Also found in part 2 is the listing of the GRAPH package, listing 1.

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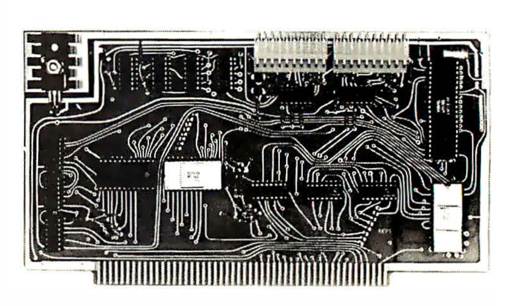
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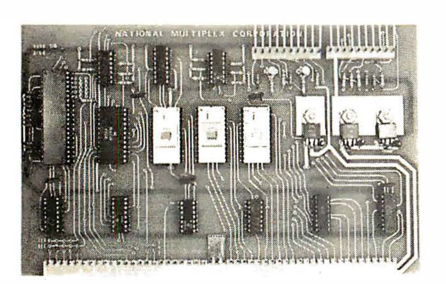
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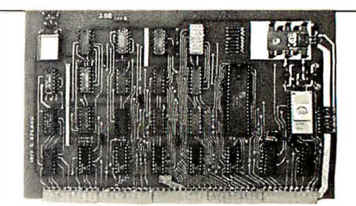
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Circle 275 on inquiry card.

A Programmable Character Generator

Part 1: Hardware

Larry Weinstein
Objective Design Inc
POB 20325
Tallahassee FL 32304

The truly critical interface in any computer system is the one that joins man and machine. One example of this is the interface between the video display and the human eye, an area where the computer outputs information at a very high rate. One way to improve this interface is to provide for maximum flexibility in the choice of characters displayed. This article presents circuitry for adding software controlled character graphic definitions to existing video display devices.

For many applications, the ability to create the characters that appear on the terminal screen is a tremendous convenience, if not an absolute necessity. The use of computers for advanced mathematical applications often requires special symbols such as Greek letters, subscripts, superscripts and variable sized fonts. APL is a good example of an advanced programming language that uses many special symbols. Computing programs that transform the general purpose computer into the equivalent of a hand held calculator suffer from the lack of a specialized keyset and the corresponding display format. Financial and scientific applications call for their own special symbols. In fact, there are very few computer applications that wouldn't benefit from easy access to a specialized character set.

Theory

The typical video display device works with a raster scan video display and produces screen characters a full line at a time. Each character is constructed on a matrix of screen dots, usually in a 7 column by 9 row configuration. The pattern for each character is stored a row at a time in a character generator, a read only memory device dedicated to this application. Before scanning past any row of a character, the character generator is accessed using the row number and character type as an address. The character type is usually the familiar ASCII code. Data produced by the character generator is shifted out serially to create the visible dots and spaces of one row of a character.

There is nothing unique about the character generator: it is merely a memory. In fact, it is becoming common for manufacturers to use large programmable read only memories in place of character generators in order to provide a programming service to customers. The size requirements of the character generator are easy to calculate. For most display purposes there is a maximum of 16 8 bit rows that could be useful for each character. There are 128 characters in the full ASCII set. The result is a memory which has eleven address bits (four for rows and seven for characters) and is eight bits wide. 2 K bytes of memory will hold all of the information in any character generator. In theory, then, it is possible to substitute 2 K bytes of vola-

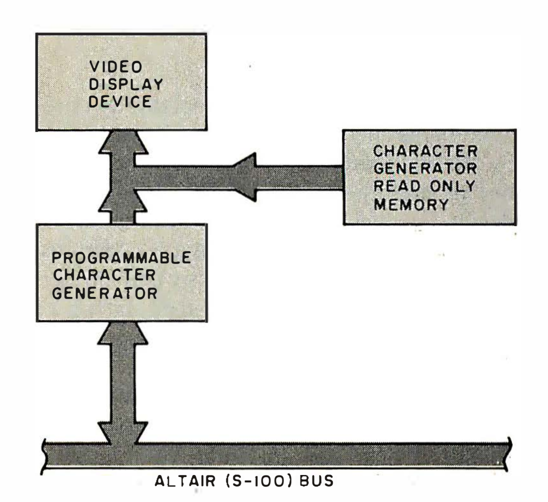


Figure 1: Block diagram of the author's graphics system, which allows the video display user to switch from conventional graphics symbols (generated by the character generator read only memory) to those generated by a programmable character generator. Special symbols such as APL characters and custom graphics symbols can be stored in this circuit and retrieved or changed at any time.

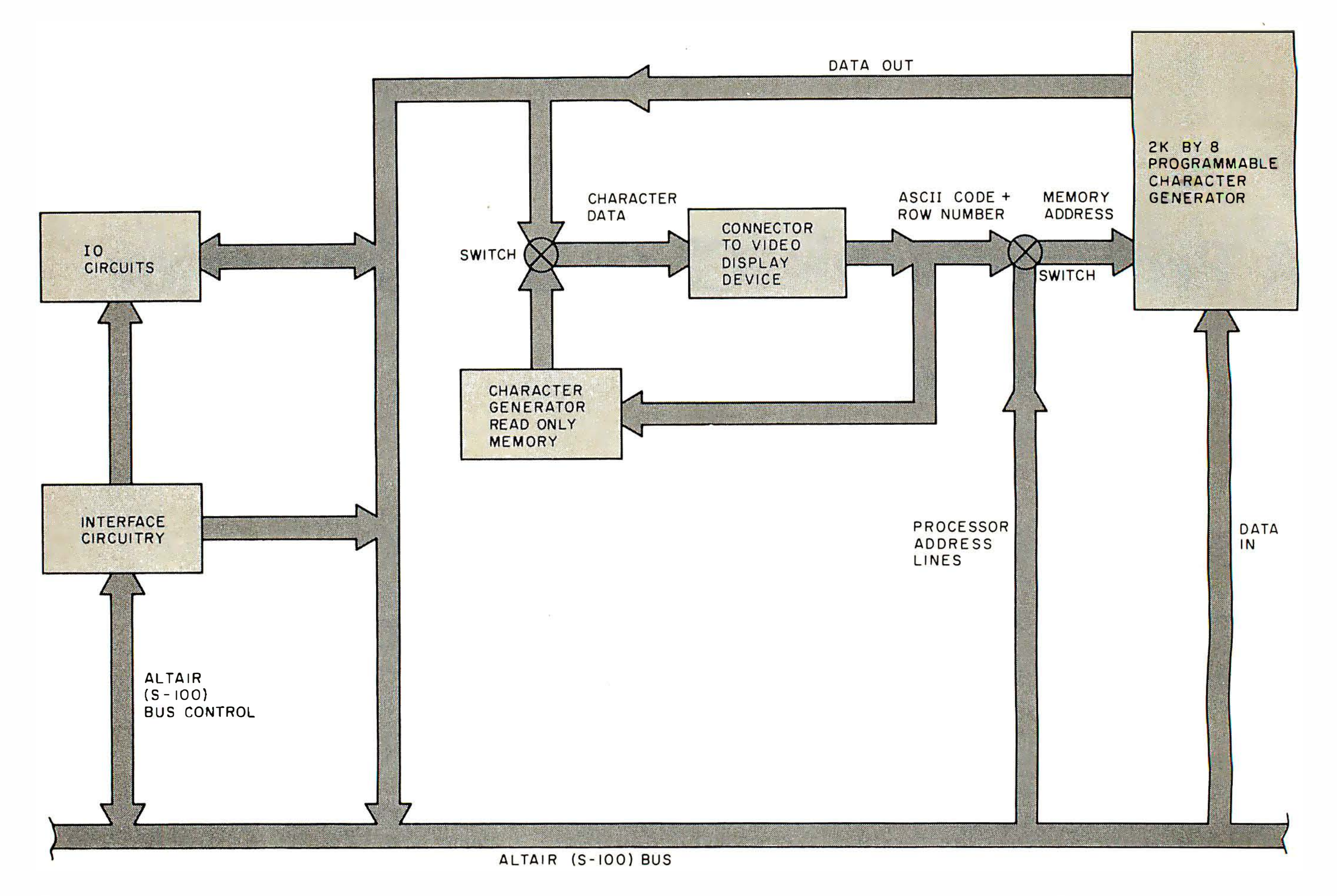


Figure 2: Detailed block diagram of the programmable character generator circuit. The circuit consists of 2 K bytes of programmable memory containing custom characters. This memory is addressed by the character and row lines that normally go to the existing character generator on the video display board. These lines are multiplexed with the normal processor address bus lines. Hardware and software switches determine whether data from the existing character generator or data from the programmable character generator will be used to feed the video display.

tile programmable memory for the character generator. This substitution of ordinary programmable memory for the character generator read only memory is the key to character graphic flexibility.

Practice

The requirements of the replacement programmable memory are that it be accessible by the main processor via its bus, and by the dot generating circuitry of the video display device (see figure 1). Retention of access to the character generator from the video display device is also desirable so that the terminal will be useable at system startup or after a software glitch wipes out a set of character definitions.

It is not difficult to gain access to address and data lines in the system: one need only construct an Altair (S-100) card interfaced to the bus. The only tricky part is obtaining access to the same lines on the video display device. This is done by substituting a 24 pin connector from the memory board for the character generator on the video display device board. The character generator is then installed in a socket on the new memory board. Through hardware and software switches, the user is able to choose between the character generator's character set and a flexible set residing in programmable memory.

Circuit Explanation

The circuit consists of 2 K bytes of programmable memory addressed by the character and row lines that normally go to the character generator (see figure 2). These lines are multiplexed with the normal processor address bus lines. The data out memory lines are available to the processor bus and are multiplexed with the character generator data lines. This data set is sent via the 24 pin connector to the video board.

During normal operation, both the memory and the character generator are addressed by row and character selection lines. Hardware and software switches determine which data set is sent to the video board for display. If the processor should require access to the memory for read or write, the processor address lines are switched in to the memory.

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GENERAL

SCREENSPLITTER is a self-contained hardware/software TV text display system for your microcomputer. It comes on a single, high-quality S-100 buss compatible board, complete with its unique Window Package software module. With the Window Package, you can logically segment SCREENSPLITTER's huge 40 x 86 display of upper-lower case characters into up to 3440 independent "windows" of various sizes. (You get the idea from our ad!) Each window has its own optional frame, cursor, figure-ground, and optional label, and each window scrolls and automatically formats its text independently of all the others. QUICK! There's some interesting information flashing by in WINDOW 1. Go read it!

WINDOW 1

▪∑∫÷∂~∈≤ι▲¶ Whoops! Our output routine seems to be having problems. Oh well, at least you get to see some of SCREENSPLITTER'S scientific symbols. (You can order a graphics character set optionally.)

▲△▲△▲△ time → And any character may be user-defined as a winking character. How? you ask. Simple: SCREENSPLITTER uses a 2708 reprogrammable memory as its character generator. Turn on the character's "wink" bit in the 2708, and presto!

Oh, and naturally, each of the 3440 characters on the screen may have its figure-ground reversed independently.

Frills, you say? No, thrills! Just take a look in the window up there ↗ to see how SCREENSPLITTER puts these raw materials to work in the onboard 1K Window Package▲ (that back there → is the cursor character).

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windows
are (it
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your te
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to one c
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you can
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THE CARE AND FEEDING OF WINDOWS

OK. You have just powered on. Initialize the Window Package and turn on your first window:

```
INIT()
OPEN(1,10,15,20,30)
```

window 1

Now, just to flex your bits, give the user a wake-up flash (a brief figure-ground reversal inside the window):

```
FLASH(1)
```

Now that you have his attention, go ahead and frame the window (you don't have to, of course):

```
FRAME(1)
```

and, while you're at it, label it, and set the scroll line count:

```
LABEL(1,"General I/O")
SCROLL(1,5)
```

(i.e., when the window fills up, pop it up 5 blank lines)

Just to keep him interested, switch the cursor character from the default caret to the winking caret:

```
CURSORCHAR(1,△)
```

Now that he's all excited, eyes bulging from the initial flash, transfixed by the hypnotic winking cursor, hit him with some text through window 1:

```
PRINT(1,"I hate to tell you this, William, but
        last night the kids wired that chair
        you're sitting in with 110 volts AC.")
```

Now (this'll really kill him), open a second window to the right:

```
OPEN(2,10,50,5,20)
FRAME(2)
LABEL(2,"Will's Will")
```

and print out a second message through this new window:

```
PRINT(2,"Please type your last will and testament.")
```

Now, of course, you echo his input through window 2, relying on the default scrolling of 1-line "pop-up" when the window fills up.

And on, and on...

PARTIAL FUNCTION SUMMARY

- INIT()
- OPEN(W,X,DX,Y,DY)
- CLEAR(W)
- FRAME(W,C1,C2,C3)
- UNFRAME(W)
- REFRAME(W,C1,C2,C3)
- LABEL(W,STR,LEN)
- LABELS(W,STR)
- FLASH(W)
- COMPLEMENT(W)
- SCROLL(W,N)
- CURSORCHAR(W,C)
- PRINT(W,STR,LEN)
- PRINTS(W,STR)
- BACKSPACE(W)
- CLEARLINE(W)
- FRESHLINE(W)
- PLOT(W,X,Y,C)
- MOVEWINDOW(W,X,Y,C)

POINTS OF INTEREST

- Entire hardware/software system on a single, high-quality S-100 buss compatible board.
- Drives a 10mhz or better TV monitor via standard 75 ohm coaxial cable (supplied).
- 4K static RAM -2114's- display buffer is memory-mapped into your CPU's address space for fast, convenient access if you ever need to bypass the Window Package software.
- User-selectable wait state for operation with 4mhz CPU's.
- 1K onboard 2708 is jumper changeable to a 2K 2716 for user extensions to the Window Package.
- Board presents one TTL load to host, yet drives up to 20 TTL loads via 74367 buffers.
- Provisions for jumpering TV data, sync, blanking off board for external mixing (via 16 pin socket).

WHAT YOU GET

- Complete SCREENSPLITTER Kit, with all IC's, low profile sockets, preprogrammed Window Package EPROM, assembly instructions
- Comprehensive Theory of Operation Manual
- Complete source-code listing, and User's Manual for the Window Package
- 90 day warranty on parts and labor

```
    +

    +

  + + +

  + + +

+ + + + +
```

the PLOT(W, X,Y,"+") thickens

ORDERING INFORMATION

1. Tell us for which 8K boundary you would like your Window Package assembled.
2. Tell us whether you want the scientific symbols, or the graphics characters in ASCII codes 0-31 of your character generator, or the optional APL character generator.
3. Send us a personal check, Master Charge or BAC/VISA number and expiration date. Kit price is $329. Assembled, $429. (Virginia residents please add sales tax.)
4. We will send you the SCREENSPLITTER, postpaid in the continental U.S., from stock to 40 days.

SOME APPLICATIONS

1. You have a BASIC program. Open a number of windows, giving each important subroutine in the program its own window. When your program runs, you get a two-dimensional feel of the flow of the execution - flurries of activity here, brief flashes there. You can have the feeling of being able to converse with each subroutine individually!
2. You have a page-oriented text editor. Pick up a paragraph here, a paragraph there, isolating each in its own window while you rummage through the main text in its own large window. Using the MOVEWINDOW function, you can move blocks of text around to produce a final layout.
3. You have an assembly language debugger. Allocate one window to the real-time clock, another to the run-time clock, and several more to display various registers in your 8080 or Z80. Then, you can keep the debugging information separate from your program's I/O, with the debugging information continually present.
4. You have some fancy games. Give each player his own window and define some "community windows." Let your imagination take over!

PS: Watch for our full graphics board, also with its own onboard software... Coming soon!

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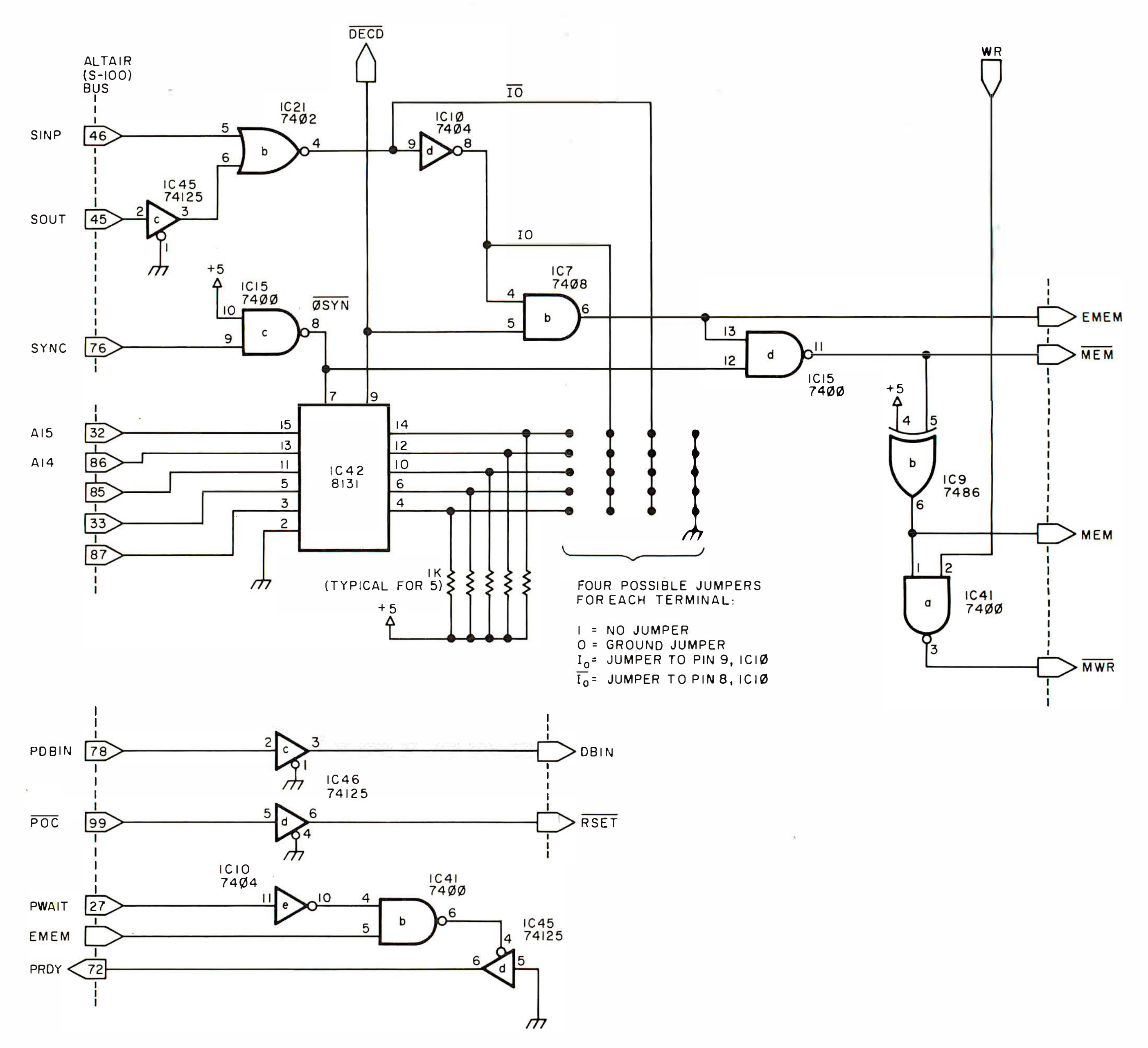


Figure 3: Programmable character generator bus interface circuitry. An 8131 (IC42) seeks for a match to the high five address lines to indicate a programmable character generator memory or peripheral action. The single 8131 can match different addresses by offering the compare circuit a choice of +, IO, $\overline{IO}$ or ground. Where the address line match for memory and peripherals is the same (either 1 or 0), a + or ground connection is used. Where they are different, the IO line is chosen if IO is 1 and memory is 0; the $\overline{IO}$ line is used if memory is 1 and IO is 0. The 8131 latch is opened during SYNC. By the time SYNC ends and the latch is closed, the match condition is determined. $\overline{DECD}$ is low on a match. If both INP and OUT are low (indicating that this is not an IO operation), the MEM signal will go high. This will cause the READY line to be pulled high, forcing a wait cycle from the processor. With the PWAIT signal, READY is brought down. All memory operations (and only memory) will have a single wait state. The MEM line is combined with DBIN and WR to produce "memory read" and "memory write" actions. There are four data select modes available on the programmable character generator: fixed, programmable, command, and automatic. In the fixed mode, the data select lines for the multiplexers are set high for normal characters and low for programmed characters. In programmed mode, the high order bit from the video display device, usually used internally for reverse video, is brought out via pin 14 on the connector to control the data select process. In command mode, the output of a flip flop determines the selection process. The flip flop can be switched by output commands. OSL-1 brings programmed characters; OSL-2 switches to normal characters. In automatic mode, the multiplexers switch to the character generator for all of the upper case set (hexadecimal 20 thru 5F), and to the programmable memory for the control characters (hexadecimal 00 thru 1F), and the lower case characters (hexadecimal 60 thru 7F).

If one is attempting to read a programmed character byte during a processor memory access, the system causes the data switch to blank the output to the 24 pin connector.

The circuit has several modes of operation. It can be hardwired via an on board switch to use only the character generator (normal mode) or only the memory (graphics mode). It can be set up to flip back and forth from graphics to normal mode by software commands. In another mode, the state of bit 7 of the character select lines will determine the mode. The final operation mode selects the 64 upper case ASCII characters (letters, numbers, and symbols: hexadecimal 20 through 5F) to come from the read only memory and all others (control and lower case: hexadecimal 00 to 1F and 60 to 7F) to be taken from the programmable memory. An 8212 on the board provides 8 bit parallel input port for interfacing a keyboard. In addition, four monostable circuits (555s) provide a simple interface for two joysticks in two dimensions. Following an output command, all the monostables fire. The length of each pulse is determined by the associated external potentiometer. A software loop is required to monitor these and produce a value for the joystick position. The remainder of the circuitry is concerned with address decoding for the processor bus. All components are standard and may be obtained from many distributors and wholesalers.

Compatibility

The programmable character generator as presented is intended to work with video display devices using the Motorola family (MCM 6574-6) of 7 by 9 matrix character generators. With a few minor changes in the connector, the circuit can be applied to display devices with other types of character generators: such as the 2513, which works with a 5 by 7 matrix. The cable may be extended as needed to connect with normal terminals. However, the best results are achieved with memory mapped video display devices such as the Processor Technology VDM-1, the Solid State Music Video Board, and the PolyMorphic Systems Video Terminal Interface. Obviously, the circuit presented can be adapted to processor interfaces other than the Altair (S-100) bus. (My personally designed and produced circuit board, available from Objective Design Inc, is Altair (S-100) compatible and designed for the Motorola series character generator.) All the aforementioned combinations of video display device and programmable character generator will produce programmable characters on the screen. In addition, certain

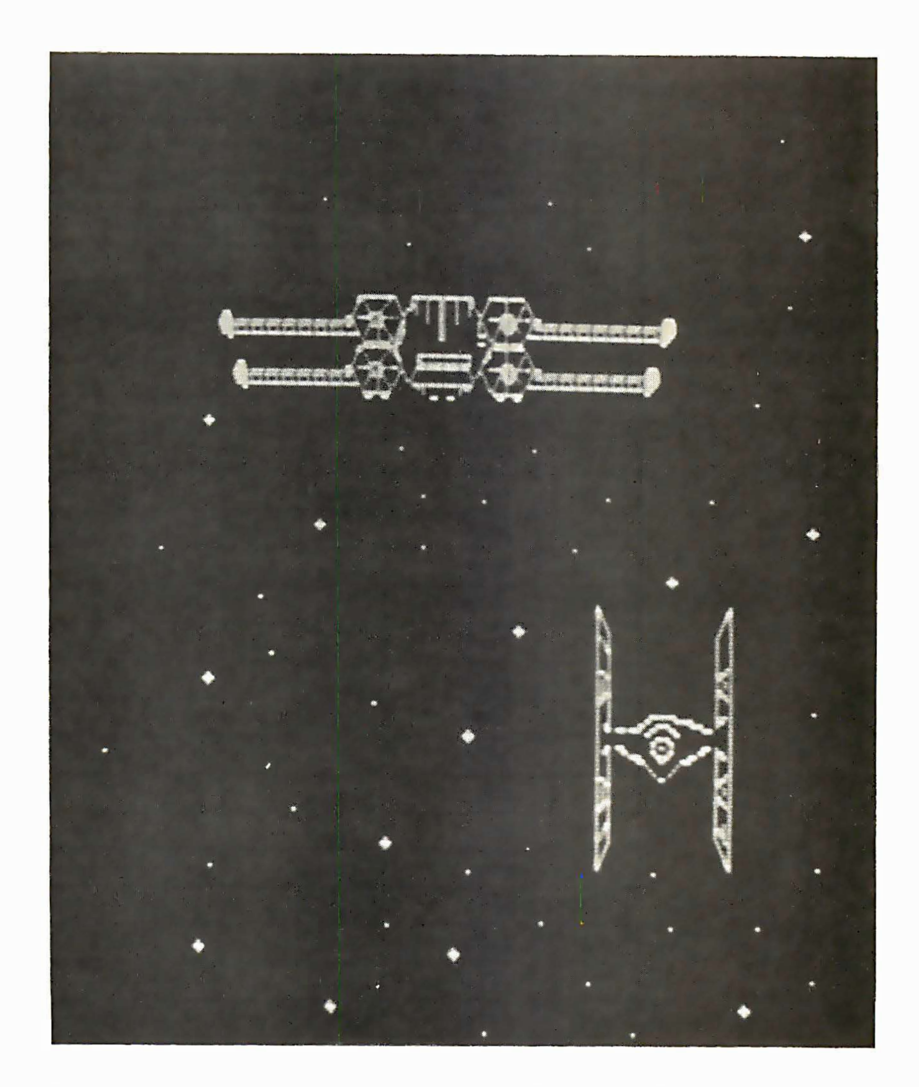


Photo 1: A Star Wars *scenario created with the aid of the author's programmable character generator and a Processor Technology VDM-1 video display board.*

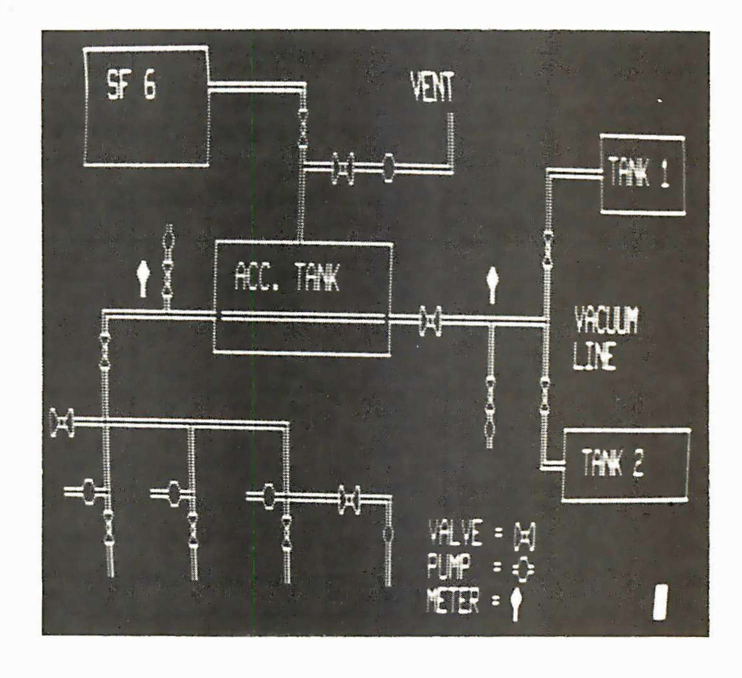


Photo 2: A piping diagram, an example of what can be done with the programmable character generator.

Table 1: Power wiring table for figures 3 thru 7.

Number	Type	+5 V	GND	+8 V	−12 V
IC1	74157	16	8		
IC2	74157	16	8		
IC3	74157	16	8		
IC4	74157	16	8		
IC5	74157	16	8		
IC6	MCM6574-6	2	13		1
IC7	7408	14	7		
IC8	7474	14	7		
IC9	7486	14	7		
IC10	7404	14	7		
IC11	8212	24	12		
IC12	74125	14	7		
IC13	74125	14	7		
IC14	74125	14	7		
IC15	7400	14	7		
IC16	7407	14	7		
IC17	555	8	1		
IC18	555	8	1		
IC19	555	8	1		
IC20	555	8	1		
IC21	7402	14	7		
IC22	74138	16	8		
IC23	74125	14	7		
IC24	74125	14	7		
IC25	21L02	10	9		
IC26	21L02	10	9		
IC27	21L02	10	9		
IC28	21L02	10	9		
IC29	21L02	10	9		
IC30	21L02	10	9		
IC31	21L02	10	9		
IC32	21L02	10	9		
IC33	21L02	10	9		
IC34	21L02	10	9		
IC35	21L02	10	9		
IC36	21L02	10	9		
IC37	21L02	10	9		
IC38	21L02	10	9		
IC39	21L02	10	9		
IC40	21L02	10	9		
IC41	7400	14	7		
IC42	8131	16	8		
IC43	7805		2	1	
IC44	7805		2	1	
IC45	74125	14	7		
IC46	74125	14	7		

applications will produce high resolution graphics for special purposes (ie: bar graphs). However, for true graphics capability (such as space ships guiding smoothly across the screen) there are some special requirements on the video display devices to be utilized.

Graphics

True graphics ability can only be added to the memory mapped video display devices which have, or can be altered to have, a matrix field no greater than 8 wide by 16 high with no forced conditions (ie: no rows or columns hardwired high or low). Unless these conditions are met, the screen will contain blank spaces which will detract from the overall appearance of any images.

None of the three video display devices previously mentioned will satisfy these conditions without some alterations. Other video display devices will not satisfy these conditions without truly major modifications.

Processor Technology VDM-1

The VDM-1 places its characters in a 13 by 8 matrix. The eighth bit in each row is forced blank by tying the high order bit of the 8 bit shift register low. (The shift register in question is used to serialize the character data.) This can be modified by removing the ground from this pin and connecting it to pin 10 on the character generator socket, which is not normally used. From the programmable character generator schematic, it is clear that the shift register will receive bit 8 from the programmable memory when it is selected. When the character generator is selected, the line is low.

The programmable character generator makes provisions for using a bit from the video display device ASCII character memory to switch between normal and graphics modes. This bit is used in the Processor Technology VDM-1 for reverse video. It is most useful when left where it is unless there is a special need for switching character sets on a character by character basis. In this case, transfer the bit to pin 14 on the character generator socket.

The VDM-1 uses 13 rows in each character. The row address sequence for each character begins with 15, 0, 1... and proceeds through ...10, 11. On 12, the counter is reset. This leaves the user with the choice of some unusual programming of the programmable memory character generator or removing the misplaced row 15. The latter can be accomplished by forcing the scan divider (IC2) in the VDM-1 to load 0 instead of 15 when given a load pulse. This will eliminate one of the blank scan lines between the character lines, which is not a serious problem in itself.

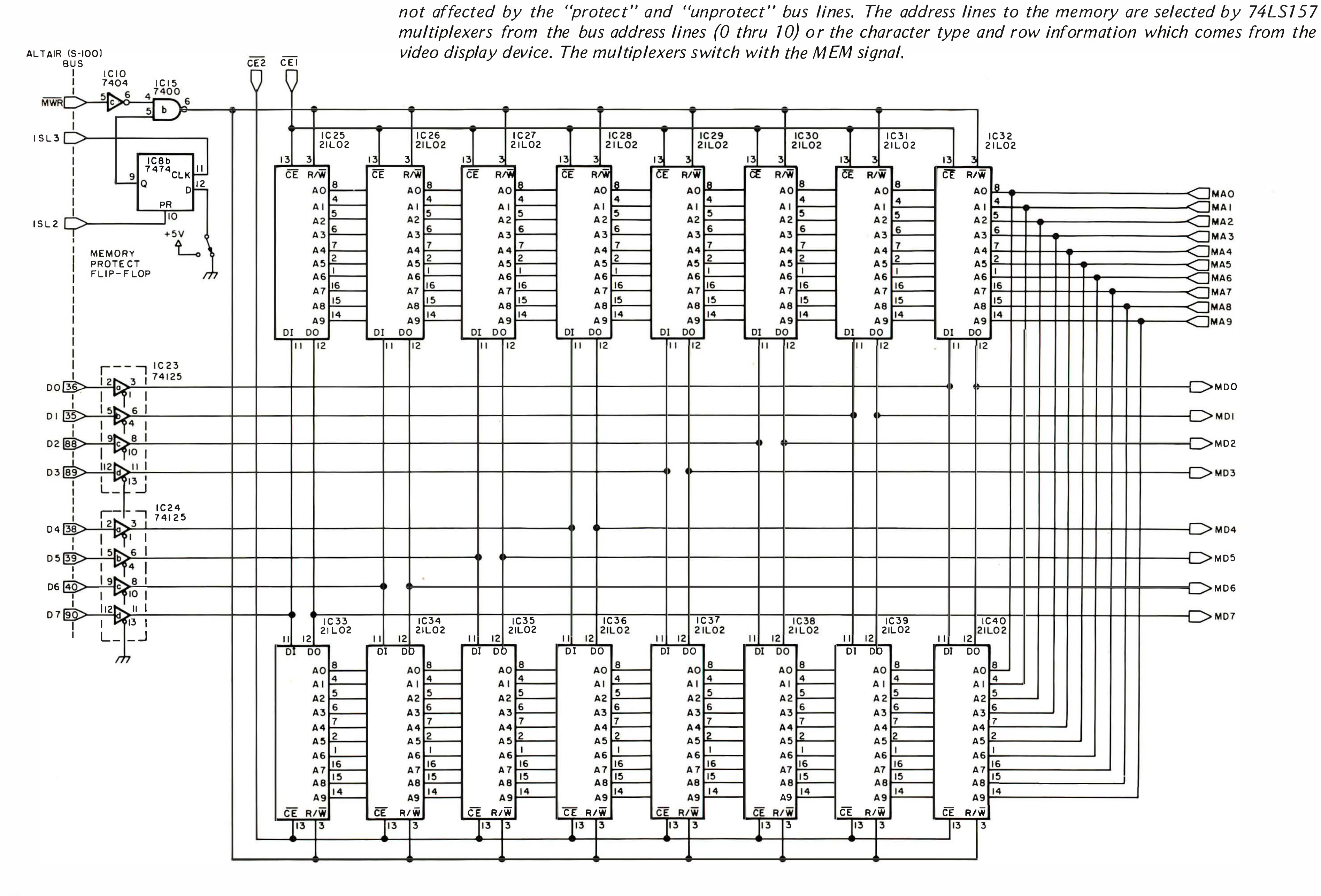
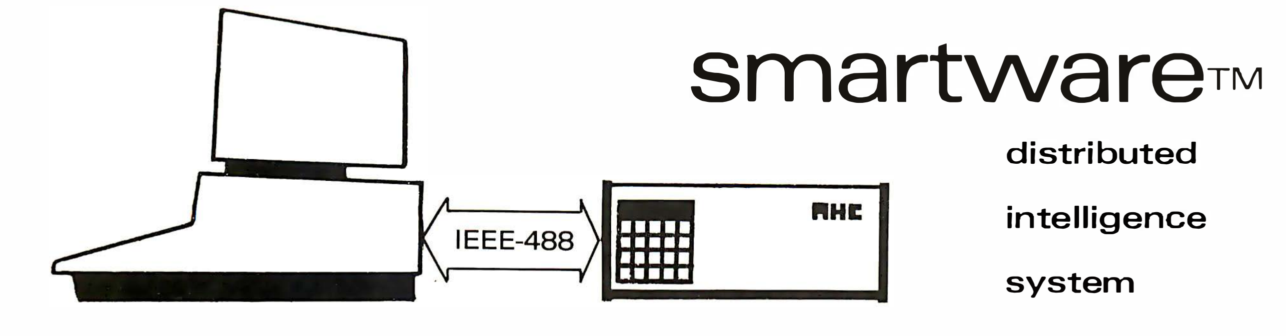


Figure 4: Programmable character generator memory circuitry. The memory consists of 16 21L02 programmable memories arranged as two 1 K by 8 banks. The memory is accessed via ten address lines (1 K bytes) and an eleventh line which activates the Chip Enable of one bank or the other. Data input is taken from the Altair (S-100) bus, buffered by three state drivers which are always on. Data output is made available to the bus via three state drivers, gated by MEM and DBIN. A memory protect flip flop provides a gating signal for memory write actions. A jumper determines whether the flip flop comes up in protect (jumper to ground) or unprotect mode with power up. The flip flop can be switched by input commands to the programmable character generator. (Data received on these commands will be hexadecimal FF.) The flip flop is not affected by the "protect" and "unprotect" bus lines. The address lines to the memory are selected by 74LS157 multiplexers from the bus address lines (0 thru 10) or the character type and row information which comes from the video display device. The multiplexers switch with the MEM signal.

Switch Settings

Mode	Switches Closed (On)	Switches Open (Off)
Fixed Normal	1,8	2,3,4,5,6,7
Fixed Special	3,8	1,2,4,5,6,7
Programmable	2,6,8	1,3,4,5,7
Command	2,4,8	1,3,5,6,7
Automatic	2,5,7	1,3,4,6,8

Figure 5: Character generation circuitry. The information which would normally go to the character generator on the video display device (seven character select lines and four character row lines) is brought to the programmable character generator via a cable and 24 pin connector which is placed in the character generator socket. The character generator is removed from the video display device and placed on the programmable character generator board. The 11 lines are sent to the programmable character generator memory by the address multiplexers. These lines are also presented to the character generator just as they are in a video display device. The output data from the memory and the character generator are both input to a multiplexer, the output of which is returned to the video display device via the cable and socket. When the character generator data is selected, the results are the same as they would have been if there were no programmable character generator involved. When the memory supplied data is selected, the video display device will produce characters whose design has been programmed.



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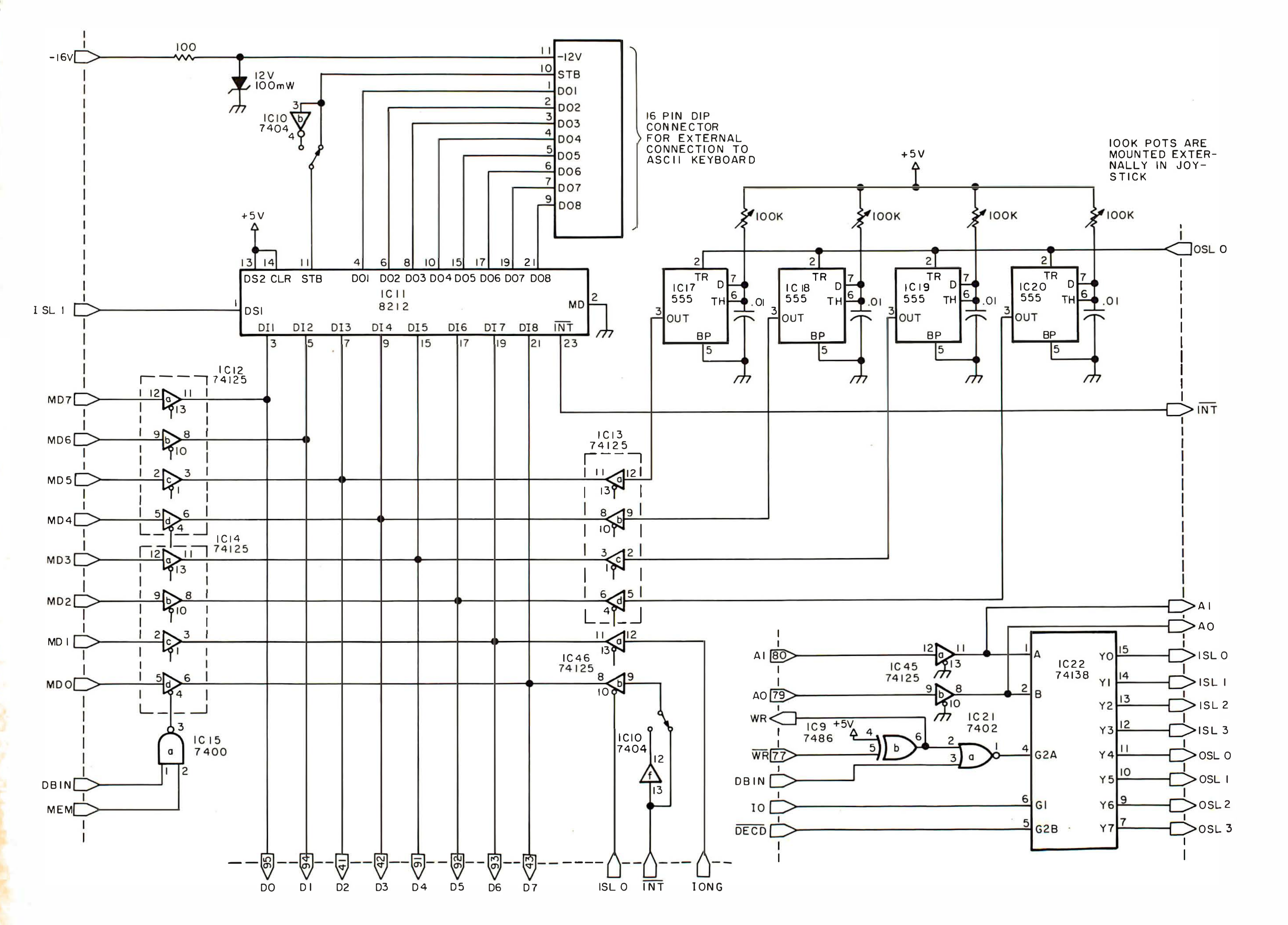
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IC13 74125
IC12 74125
IC14 74125
IC15 7400
IC10 7404
12V 100mW
100K
.01
100
+5V
-16V
I SL 1
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
DBIN
MEM
D0
D1
D2
D3
D4
D5
D6
D7
ISL 0
INT
IONG
A1
A0
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DECD
IO
OSL 0
OSL 1
OSL 2
OSL 3
ISL 1
ISL 2
ISL 3

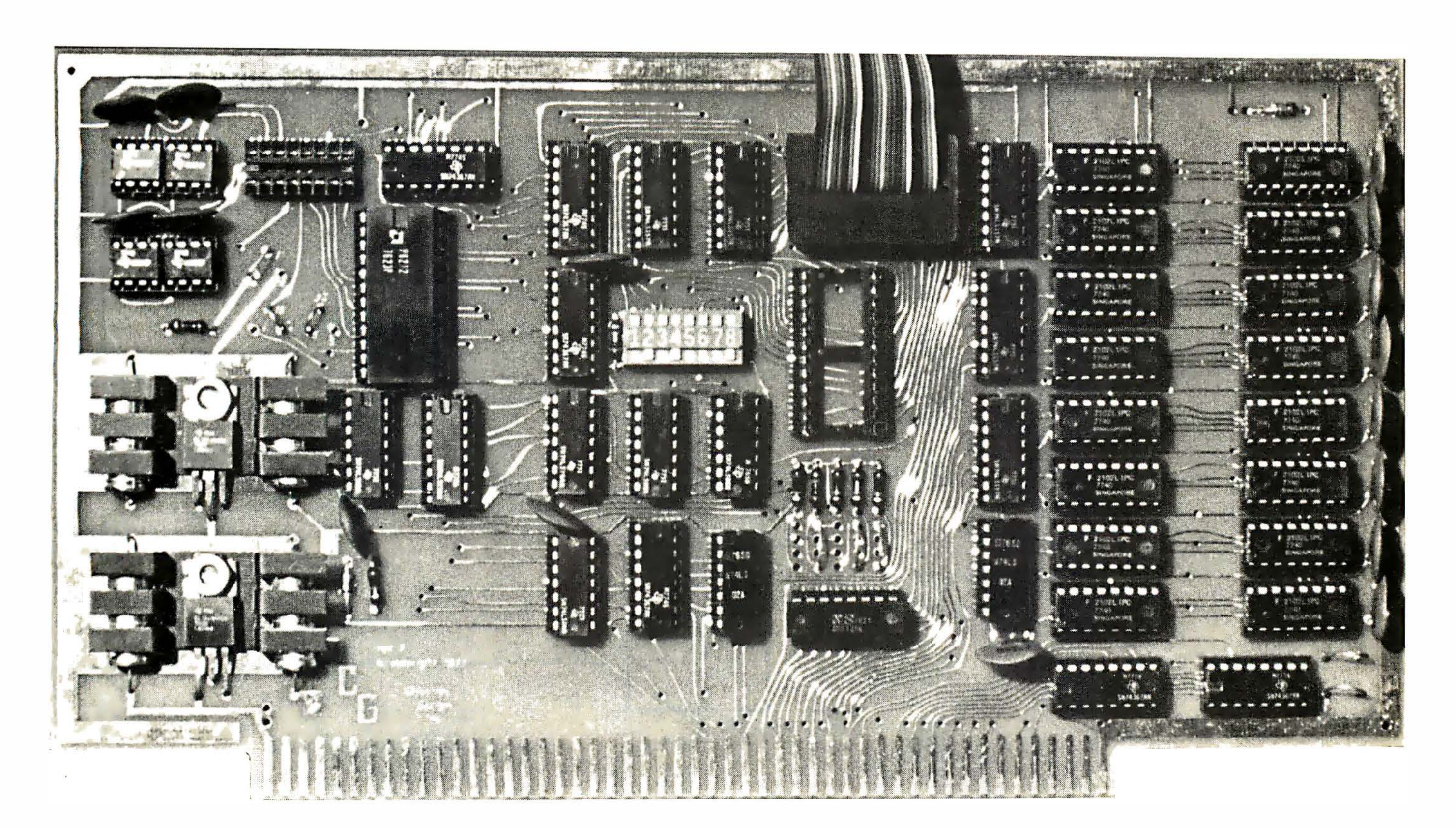


Photo 3: *The programmable character generator board.*

←

Figure 6: Programmable character generator IO circuitry. A 74LS138 3 to 8 decoder is gated by $\overline{DECD}$, IO, and the OR combination of WR and DBIN to produce eight IO strobes. The OUT signal is used as the most significant address bit, splitting the output into four input and four output signals. An 8212 (made by Intel) is used to implement an 8 bit parallel input port and data available signal. The data available flag can be read with ISL-0 (bit 0) and can be wired ready-high or ready-low. The data is read with ISL-1. Four monostables made with 555s connect to external 100 k ohm potentiometers to provide a simple joystick interface. The monostables are triggered in parallel by OSL-0 and remain high for a time dependent upon the external resistance value. The timing range is from 100 µs to 1000 µs. Users must time the pulses with software loops or real time clocks while monitoring the outputs via ISL-0, bits 2 thru 5. OSL-1 and OSL-2 will switch the select flip flop, and ISL-2 and ISL-3 will switch the memory protect flip flop. Finally, ISL-0 bit 1 provides a look at the character data select line. This data is valid only for the fixed and programmed modes, since the line is switching in the programmed and automatic modes in a manner not synchronized with processor commands.

Label	Operator	Operand	Commentary
INIT	LXI	B,0	CLR COUNT
	LXI	D,0	CLR COUNT
	OUT	OC1H	TRIGGER
CHK	CALL	DELAY	100 MICROSECONDS
	IN	OC3H	MONO INPUT
	RRC		
	RRC		
	ANI	OFH	TEST MONO FLAGS ONLY
	ORA	A	
	JZ	REPRT	ALL DOWN, REPORT
	RRC		TEST FIRST
	JNC	*+1	NC – DOWN
	INR	B	STILL UP, COUNT
	RRC		
	JNC	*+1	
	INR	C	
	RRC		
	JNC	*+1	
	INR	D	
	RRC		
	JNC	*+1	
	INR	E	
	JMP	CHK	CONTINUE COUNTING

Listing 1: Joystick interface test program. A single output command triggers all of the monostables. The user must time each one with software. In this simple program the count for each timer is maintained in a register. On each pass through the loop, the register is incremented if its associated monostable flag is still high. When all four have come down, the loop ends and the values are reported to whatever routine has requested them. The DELAY subroutine called is a 100 µs time user. The length of time delay used is determined by the R and C combinations in the hardware and the range of counts for which the software is prepared.

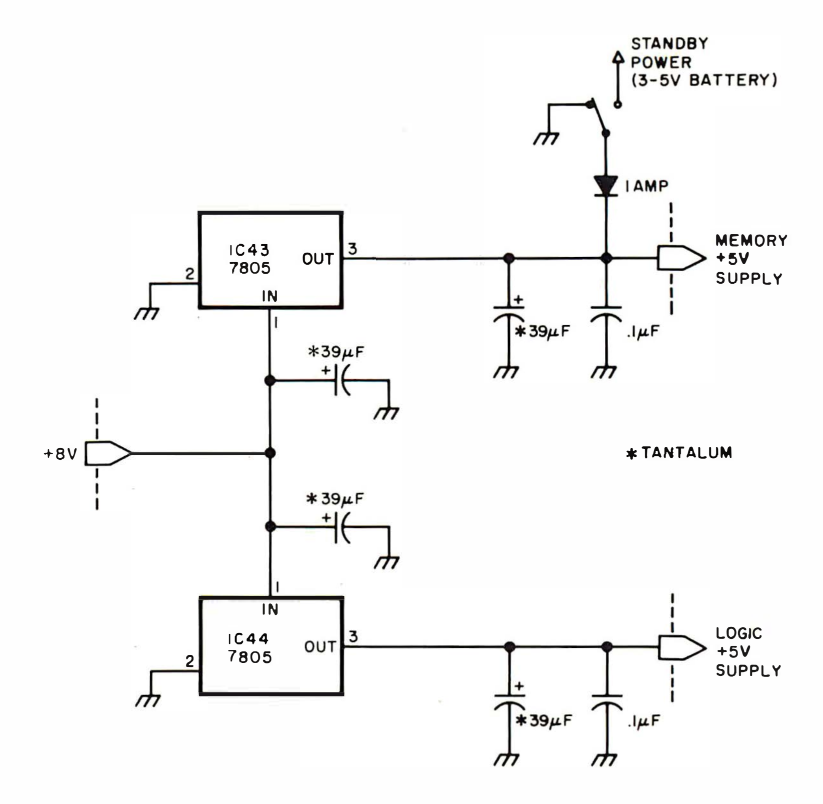


Figure 7: Programmable character generator power circuitry. +5 V for the logic and memory circuitry is provided through separate 7805 or 340-T5 regulators, properly heatsinked. Standby power for the memory is provided via a 1 A diode. A 3 to 5 V battery backup should be connected to the board to use this feature, and suitable supply filtering at the regulators and on the board should be provided. The low current −12 V required by some keyboards is generated by a simple resistor and zener diode combination.

The overall absence of 16 scan lines will force some adjustment of the vertical size and linearity of the monitor.

PolyMorphic VTI

The PolyMorphic VTI uses an unusual 15 by 10 matrix. The 15 rows will cause no problems for graphics, but the ten dots per row will cause problems. Seven of the ten dots in the row come from the character generator socket. The other three are forced blank. The problem is further complicated by a 10 bit shift register which shifts out the blank dots first and the VTI "block graphics" circuitry. Obviously, the change to this circuit is not simple. It is recommended that the 74LS157 multiplexers (ICs 35 and 32) be removed and replaced with dual in line package component carriers with jumpers to connect the 8 dot bits from the character generator to the rightmost bits (2 thru 9) of the shift register. To insure that only eight dots are output per character, it will be necessary to change the load number on IC14 from 6 to 8.

Of course, the usual graphics ability of the VTI is lost in the conversion, but these, plus many more characters, can be duplicated with the programmable character generator. (Note: Modification of the VTI circuit should not be attempted without complete knowledge of the details of the VTI circuit.)

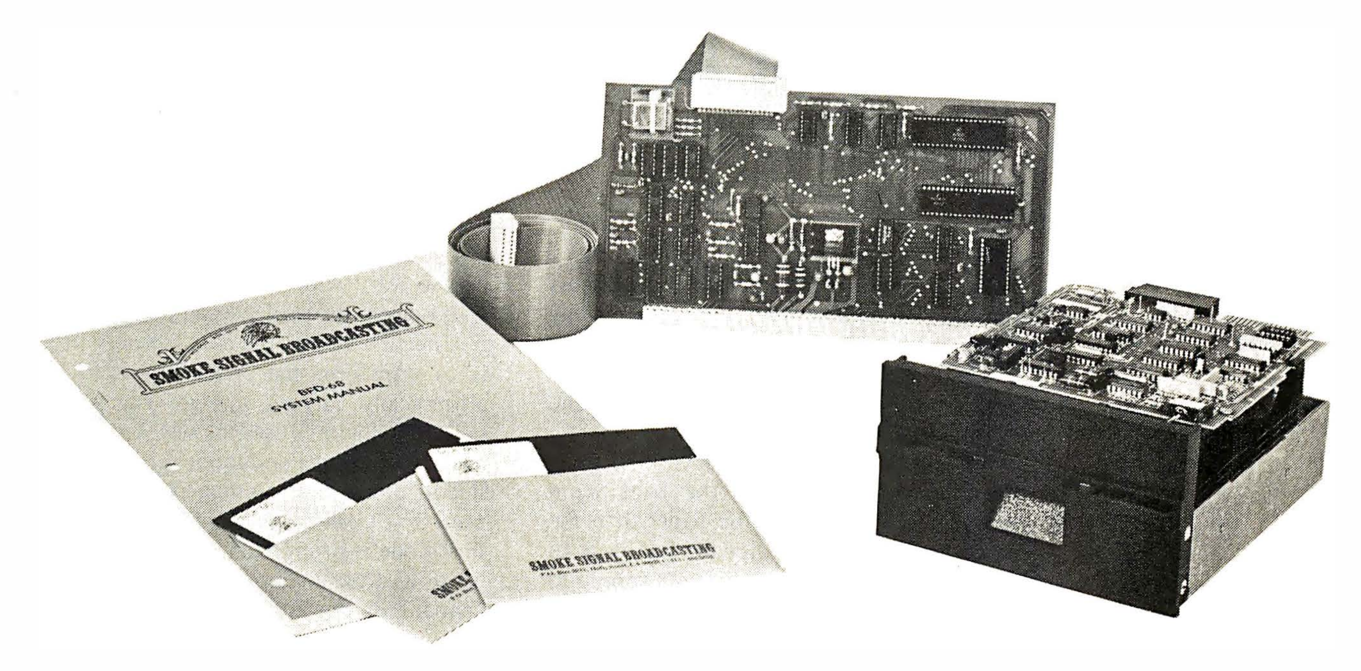
Software

Once the programmable character generator and video display device are joined, the software must take over. Details on the use of the programmable character generator along with some sample programming will be described in part 2 of this article.■

Note: The programmable character generator described in this article is available from Objective Design Inc, POB 20325, Tallahassee FL 32304, in the following configurations:

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A Low Cost Light Wand Amplifier

Robin C Moseley
14 Standish Circ
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The purpose of this article is to discuss some of the variables involved in the reading of printed bar data, and to describe a signal processor whose operation is independent of most of these variables, and tolerant of the remainder.

For the most reliable recovery of data, the effective aperture of the light wand photodetector should be no wider than the narrowest data bar. In this case, full black to white signal swing is obtained in response to narrow bars, and variables such as lamp output, photodetector sensitivity, pen angle, and target contrast control only two output functions: white level photocurrent and black level photocurrent.

In any light wand having a linear photodetector, the ratio of these currents is determined by the ratio of the reflectivities of the black and white bars, ie: target contrast. The absolute value of the photocurrent may, of course, vary widely between different light wands, even those of the same design.

The first step in the data recovery process is to transform the photocurrent to a logarithmically varying voltage. The amplifier shown in figure 1 uses the well known exponential forward conduction properties of a silicon diode (D1) to make this transformation. The peak to peak signal voltage across this diode is proportional to the ratio of the white and black photocurrents and is independent of the absolute level of the photocurrent.

The next step in processing the signal is to eliminate the effect of the variation of the absolute level of photocurrent. This is most obviously achieved by capacitively coupling the signal developed across the diode. This method results in unwanted transient shifts of signal level at the output of the amplifier when the light wand is first placed on the

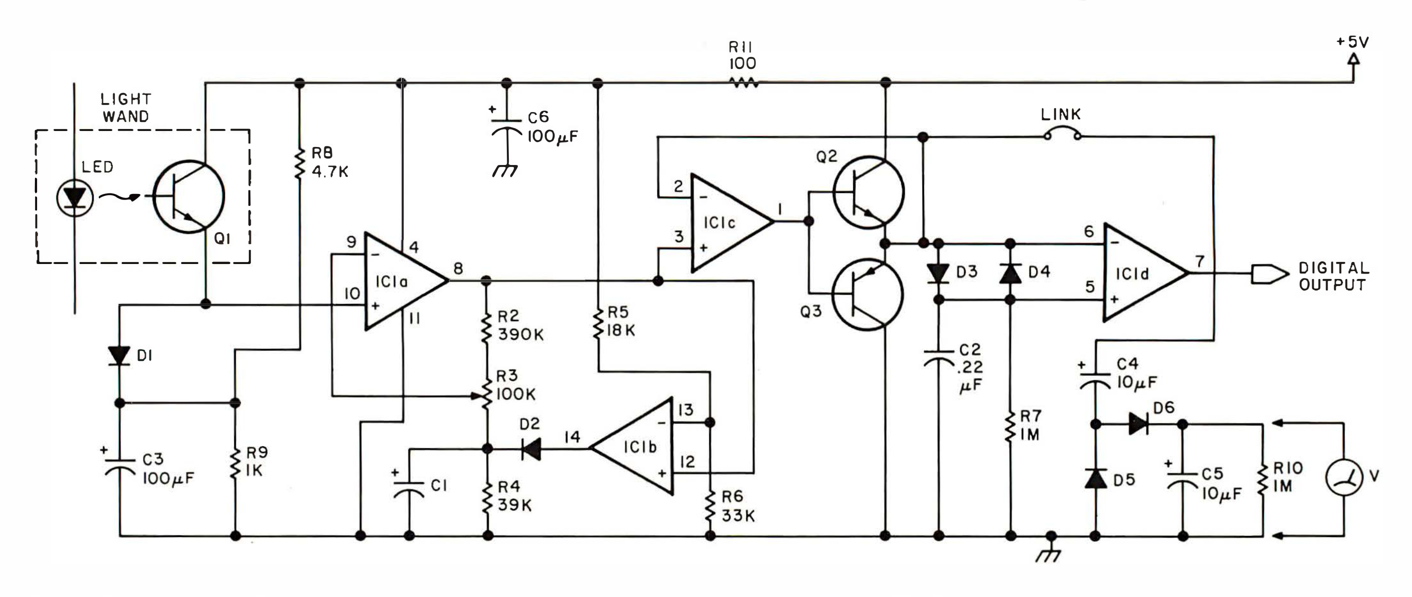
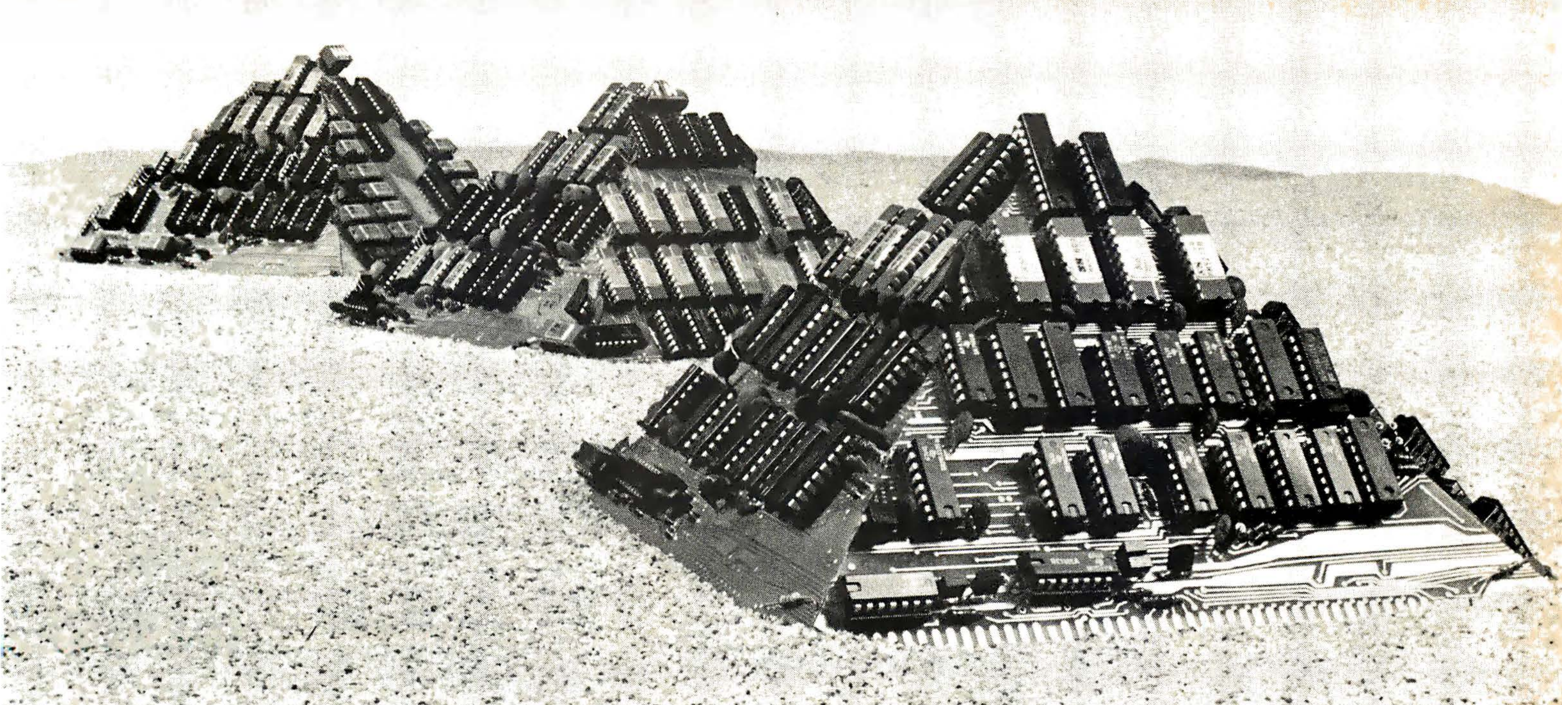


Figure 1: Schematic diagram for light wand signal processor. IC1 is a National LM324 quad operational amplifier. All the diodes are general purpose silicon diodes such as 1N4148. Q2 is a general purpose NPN transistor such as MPS6513 and Q3 is a general purpose PNP transistor such as MPS6517. All resistors are 0.25 W and all resistances are measured in ohms. The output of the circuit is TTL compatible.



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white margin of the printed data and also at the beginning of the data track. Provided the dynamic range of the amplifier is sufficient to accommodate these shifts, the decision threshold circuit described below will compensate for them. A more elegant approach, however, is to borrow from television technology and clamp the white level output from the amplifier stage at a fixed level. This is the function of comparator A2 and peak detector D2, C1.

Before the light wand is placed in contact with the printed data, the photocurrent is small. The output voltage of amplifier stage A1 rises until it is equal to that at the other input of comparator A2. At this point, the output of A2 goes high, charging capacitor C2 until the voltage across this capacitor is approximately equal to that at the anode of logarithmic converter diode D1. When the light wand is placed in contact with the white margin of the data, the photocurrent increases. As the output level of the amplifier tries to rise, comparator A2 output switches high. This rapidly raises the reference voltage level across capacitor C1 to a new, higher level corresponding to the white level voltage at the anode of D1. As the wand moves over the black bars, the reduced photocurrent causes the voltage across D1 to fall. The output voltage from the amplifier falls below that at the other input to the comparator, and the comparator voltage falls to zero, cutting off charging diode D2. Since the time constant determined by C1 and R4 is long by comparison with the signal period, C1 holds the bias input to the amplifier stage approximately constant until the next peak white signal "tops up" C1.

The peak white level of the signal at the output of the amplifier is fixed at a predetermined voltage (about 3.25 V in the design described here) and the signal swing is negative from that point. The peak value of the signal depends only on the contrast ratio of the data bars. Gain control R3 should be adjusted to set the peak to peak signal swing to the optimum value; between 1.5 V and 2 V. In the absence of an oscilloscope, optional components D5, D6, C4, C5 and R10 form a peak detector which may be used in conjunction with any reasonably high impedance voltmeter to make this adjustment. Switch the voltmeter to the appropriate DC voltage range and connect it across C5. To prevent any distortion of the signal during actual use, disconnect the peak detector from the output of the buffer amplifier except when adjusting the amplifier gain.

The final step in processing the signal is to convert the amplified and clamped signal to the binary output required by the microprocessor. My approach avoids the complexity of decision circuits which rely on multiple peak detectors to determine the decision threshold while allowing variations of contrast ratio. The threshold is set a fixed voltage above (or below) the immediately previous peak signal level. With the wand in contact with the white margin, diode D3

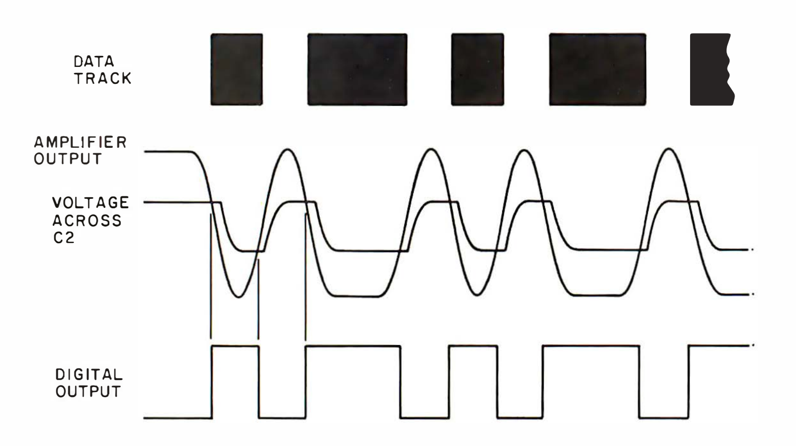


Figure 2. Sequence of events when the light wand is moved across a series of light and dark data bars. In this format the size of the black bars are changing and the size of the white spacings in between remains constant.

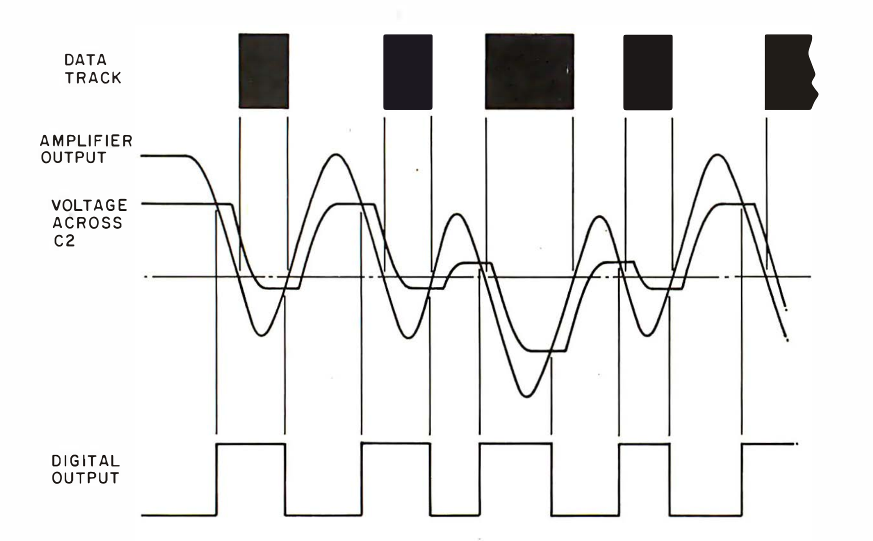


Figure 3. When the black and white bars are smaller than the aperture of the light wand it is still possible to have the correct output. The width of the digital pulses will change but will still be readable.

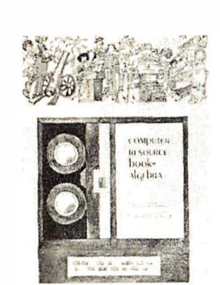
conducts, and capacitor C2 is charged to a voltage one diode drop (about 0.6 V) below the white level output from the amplifier. As the wand moves over the first black bar the amplifier output voltage falls, and diode D3 is cut off. When the output voltage falls to the same level as that across C2, the output from the comparator A4 switches to maximum (about 3.5 V). As the signal continues to fall, diode D4 conducts, and the voltage across C2 follows the signal except that it is now one diode drop more positive. As the wand moves onto a white bar, the signal voltage rises, and diode D4 is cut off. When the signal rises to a value equal to that across C2, the output of the comparator A4 falls to ground. As the signal continues to rise towards the white level, D3 conducts and the voltage across C2 follows. This time it is one diode drop less positive than the signal. Unity gain buffer stage A3 and transistors Q2, Q3 provide a low impedance drive to the decision circuit to ensure that the charging and discharging of capacitor C2 does not distort the signal at high reading speeds. The sequence of operation of the circuit is illustrated in figure 2. Notice that the digital output of this circuit follows the usual convention of a high level for black, and a low level for white. If this is not convenient, the two inputs of comparator A4 may be interchanged.

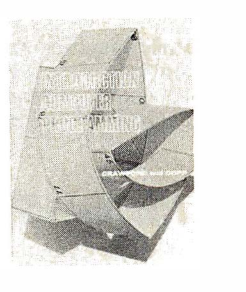
While this signal processor was designed primarily for the situation in which the effective aperture of the photodetector is no wider than the narrow data bars, it will perform creditably when the data is narrow by comparison with the detector. In this case, illustrated in figure 3, some timing error is theoretically introduced. Fortunately, this error is quite systematic; the first narrow bar following a wide bar is widened by 20% to 30% of its width, and the first wide bar following a narrow bar is reduced in width, by 10% to 20%. Some software complication is required to accommodate this. Note, however, that these comments do not apply to the case where the aperture of the photodetector is no wider than the narrow data bars; in this case the digital output from the processor is an accurate replica of the data bars.

The construction layout required for this circuit is not critical; just ensure that the low potential ends of C1 and C3 are connected closely together, along with that of the power supply decoupling capacitor C6.■

A Bit of the BASIC

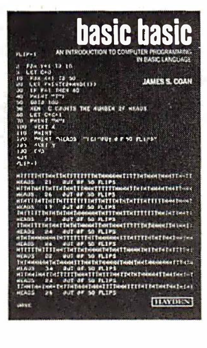
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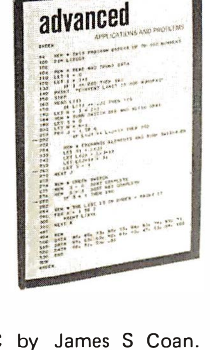




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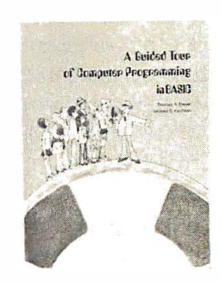
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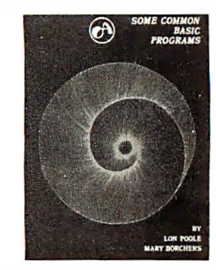




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Photo 1: The finished prototype receiver board.

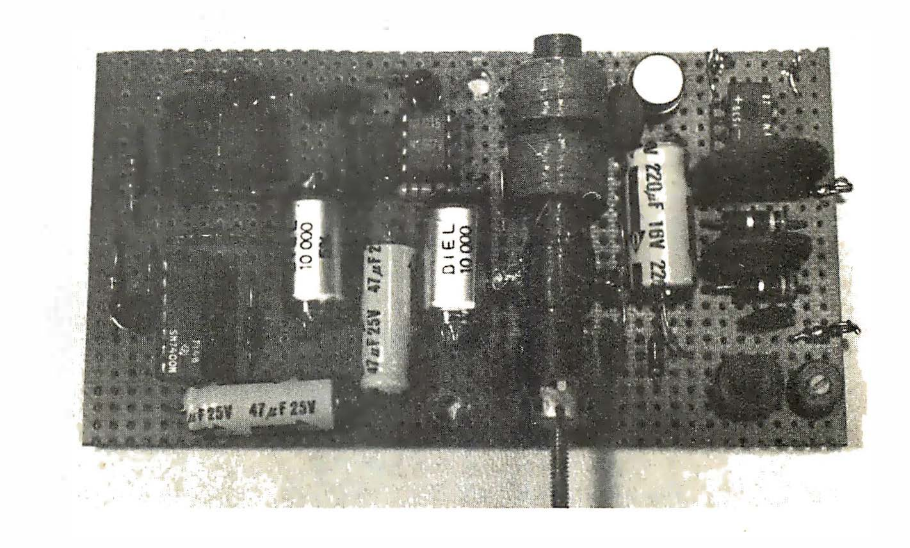
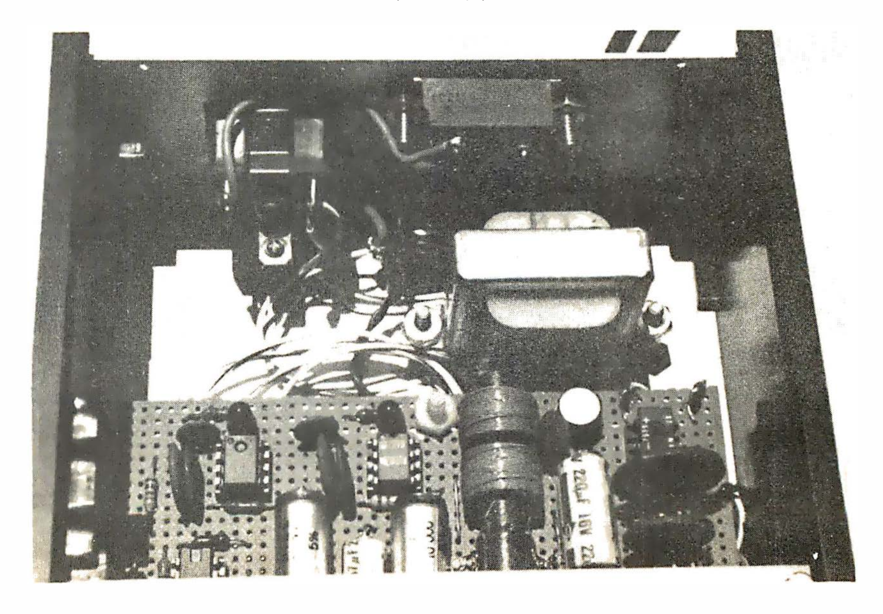


Photo 2: Internal view of finished prototype receiver chassis.



Last month (page 114) I outlined the transmitter section of a wireless AC remote control system that can be easily attached to any computer with an 8 bit parallel output port. As previously stated, it will allow remote on and off control of up to ten AC powered devices. This month I cover the design of a typical receiver section.

Figure 1 shows the schematic of a single channel receiver station and photos 1 and 2 illustrate a typical layout of a constructed receiver. (A photo of the completed receiver is shown in last month's article.) The receiver consists of three basic sections: input filter and power supply, on and off tone detectors, and output latch. Except for minor component value differences necessary to change the channel frequencies, all receivers will have the same configuration.

Input Filter and Power Supply

Each receiver, designated as a single channel, receives two transmitted frequencies from the computer. One is used to turn the AC device on and the other to turn it off. These two tones must be close enough to be passed through the same filter section but not close enough to interfere with each other. For this reason, a channel bandwidth has been designated to be 8 kHz, and no two tones are closer than 4 kHz.

The function of the input filter is to reject the 60 Hz line frequency and all other frequencies except the 8 kHz band of a specific channel. While this may appear true in theory, it is not quite the result. Instead, the amplitudes of various frequencies will be affected as they pass through the filter.

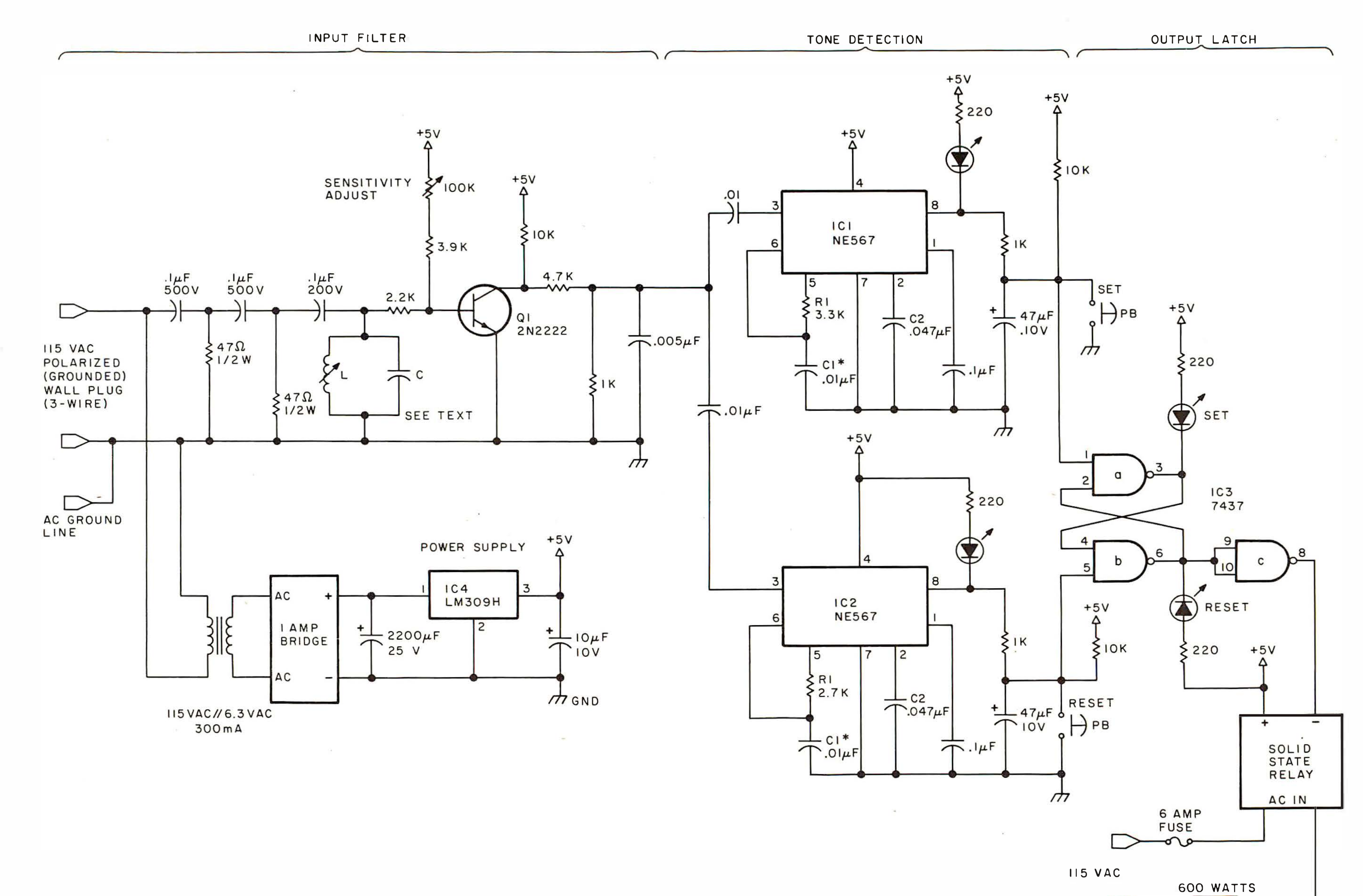


Figure 1: The receiver portion of the author's AC wireless remote control system. The user plugs an appliance or light into the receiver, which in turn is plugged into a wall socket. One of two frequencies is sent at a time through the house wiring by a separate computer controlled transmitter (described last month). The receiver responds to these frequencies by turning its device on or off, respectively. A specially designed tuned bandpass filter amplifies only that pair of frequencies dedicated to its receiver, attenuating all other frequency pairs. After some amplification, the signal is sent to two tone decoders (IC1 and IC2) which respond to the two frequencies independently. Two buttons are also present on the receiver so the user can operate the device locally. Note that the use of a 3 wire grounded plug to connect to the AC line is highly recommended.

60 Hz will be virtually nonexistent, and if the passband is from 35 kHz to 43 kHz, that frequency range should be the highest amplitude. This amplitude variation across the spectrum can be facilitated somewhat by the addition of a tuned inductance and capacitance (LC) circuit, called a bandpass circuit. The center frequency of the LC circuit should be set for the center of the particular passband desired. In the case of 35 to 43 kHz, the inductor and capacitor are chosen to produce a resonance at 39 kHz: the result is a passive filter. As the RC section passes frequencies close to 39 kHz, the LC combination starts to resonate (which increases the overall amplitude seen at the base of Q1). In practice, a low Q slug-tuned 1 to 10 millihenry coil salvaged from an old TV set will work well. By using this LC circuit, the fundamental frequency of the transmitted waveform is sufficiently high in level to be differentiated from the second and third harmonics also present. A sensitivity adjustment on the base of transistor Q1 aids in the detection process by allowing only signals of sufficient amplitude through the next amplifier filter section of Q1.

The use of an LC filter does require some component value changes to cover the 30 kHz to 110 kHz range of the transmitter. Figure 2 is the schematic of the LC combination in question and includes the formulas required to make this calculation. Again, calculations are only part of the answer and are acceptable only in 2 or 3 channel applications. For optimum tuning, the component values should be chosen according to the equation. Then using an oscilloscope, measure the voltage across the LC circuit and slowly adjust the slug-tuned coil to peak at the desired frequency. A voltmeter on the AC setting will not respond sufficiently; only an oscilloscope with high impedance inputs should be used.

The power supply section is a standard rectifier and 3 terminal regulator supply. The circuit requires less than 100 mA and values are not critical. The LM309 voltage regulator is the plastic TO-5 packaged version of the standard LM309K, which is a TO-3 metal can. Either can be used and no heat sink is required.

Table 1: Power wiring table for figure 1.

	IC Type	+5 V	Gnd
IC1	NE567	4	7
IC2	NE567	4	7
IC3	7437	14	7
IC4	LM309	3	2

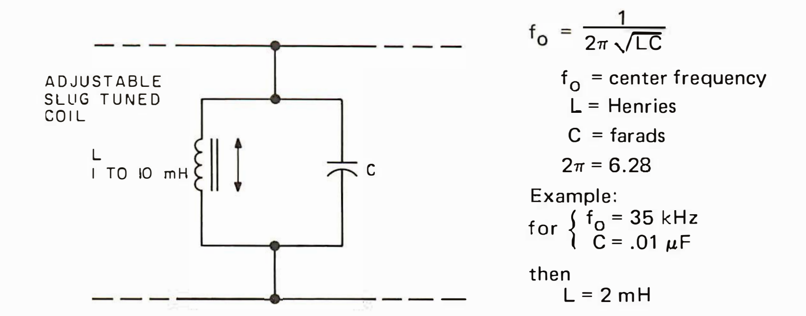


Figure 2: Calculation of inductor and capacitor values for the tuned bandpass filter used in the receiver's input section.

Tone Detectors

The heart of the receiver is in the two tone detectors, IC1 and IC2. Each is tuned to a specific frequency or tone within its respective channel bandwidth. For the channel 1 frequencies I have chosen (35 kHz to 43 kHz), IC1 would be set for approximately 35 kHz and IC2 would be set 4 kHz higher at 39 kHz. IC1 is considered the set frequency receiver and IC2 is the reset receiver. LEDs are attached to their outputs to facilitate tuning. These lights will light only when the correct frequency is present at the respective pin 3.

As with the input filter, these are tuned circuits and they require component value changes for the different channels. Figure 3 shows an individual receiver and outlines the equations used to select components. The values I have chosen are standard and could be set closer with the addition of trim pots, etc. In practice, this won't be necessary unless all ten channels are to be constructed.

Output Latch

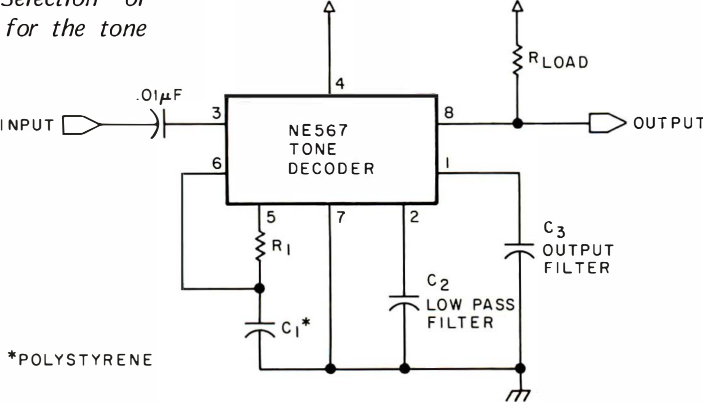
The outputs of the set and reset tone detectors go to the set and reset flip flop made from two NAND gates (IC3a and IC3b). If either the set pushbutton is pushed or IC1 receives the proper signal, the flip flop goes into the set state and the output device is activated. It will stay in the "on" condition until either the reset pushbutton is pushed or a reset signal is received through IC2.

Notes for Figure 1.

The solid state relay noted in the schematic can be either a Sigma 226 RE1-5A1 as shown in photo 1 or the homebuilt unit of photo 3 and figure 4. Minimum current rating should be 6 A.

1. All resistors 1/4 W carbon 5% unless otherwise noted.
2. All capacitors are 100 V ceramic unless otherwise noted.
3. The values of L and C in the tuned filter are computed for the particular center frequency chosen (see figure 2). In general L should be an adjustable slug tuned in a range of 1 to 10 mH. C will range from .001 to .01.
4. If this receiver is used on AC lines which also power many inductive devices such as motors and pumps, voltage surge protection may be required on the input.
5. A 7400 can be substituted for the 7437 if the set and reset LEDs are eliminated.

Figure 3: Selection of components for the tone decoder.



Example:
for $R_1 = 3.3$ k and $C_1 = .01$
$f_o = 33.3$ kHz
with $C_2 = .047\ \mu F$
Bandwidth ≅ 1600 Hz
$C_3 = .1\ \mu F$

1. Select R_1 and R_2

$$f_o \cong \frac{1.1}{R_1 C_1}$$

f_o = detection frequency (Hz)
R_1 = ohms ($1 \text{ k} \leq R_1 \leq 20 \text{ k}$)
C_1 = farads

2. Select bandwidth of less than 2 kHz for each frequency. For input amplitude ⩾ 200 mV

$BW \cong f_o C_2$
f_o = detection frequency (Hz)
$C_2 = \mu F$
BW = bandwidth (Hz)
and:

3. $C_3 = 2\ C_2$ minimum

Although the 7437 is quite capable of driving a silicon controlled rectifier (SCR) directly, turning on a triac is a bit more involved. When the parts necessary to perform this function cost more than a commercial solid state switch, it's time to go commercial. There are experimenters who will want to use SCRs because they have them, though.

Figure 4 is a schematic of an alternate 1000 W solid state relay; photo 3 is the prototype I constructed as an example. It is important to note that, while both the SCR and homebrew device in figure 4 are opto-isolated devices, the AC remote receiver itself is not isolated, and care must be taken when probing into a plugged-in unit. In this case, the only advantage of the opto-isolator is that it provides the required current to drive the SCR or triac; a 7437 by itself may not. SCR gate currents have a wide variation (1 to 100 mA for various SCRs all rated for 8 A) and a 7437 does not have unlimited drive capability. For some less current consuming applications, a standard 7400 can be used instead of a 7437.

System Checkout

There are two ways to calibrate this system: trial and error (good for one or two channels only); or with the proper test equipment (necessary for three or more channels). I prefer the latter and will discuss that technique.

The first thing to do after building the transmitter is to determine what frequencies are being transmitted. Using the program in listing 1 and a frequency counter attached to pin 6 of IC3 on the transmitter board will aid calibration. The frequency output of the transmitter described last month will have 256 possible values but not all are required at this time. A program could be written to scan slowly across all frequencies and stop when the receiver picks it up. This method involves trial and error. I prefer to tune the transmitter to a known frequency, then tune in the receiver.

Once the transmitter is set up, the next project is the receiver. For reasons I'll describe later, it is best to plug the transmitter and receiver into the same wall socket initially (use an extension cord if necessary). Using the previous program, set the transmitter to continually transmit one tone in the center of a channel, such as for channel 1 (39 kHz). Choose component values from figure 3 (figure 1 is configured for channel 1) and adjust the coil slug until the maximum voltage appears across the LC circuit in the filter section. Reset the frequency transmission for the set frequency (35 kHz) and adjust the sensitivity pot until the LED at pin 8 of IC1 comes on. Failure of the LED to light indicates any of the following:

1. Insufficient transmission amplitude: check transmitter output.
2. Wrong frequency transmitted or wrong components chosen for the receiver: check program action and recheck calculations.
3. Sensitivity pot misadjusted: attach scope to collector of Q1 and note that sensitivity pot turns signal on or off.
4. Bad tone decoders.

Once this phase is completed, set the transmitter frequency to the reset frequency (43 kHz) by entering the appropriate number when running the program of listing 1. Then check to see that the LED on IC2 lights. The sensitivity pot may require adjustment. The key is to find a setting that

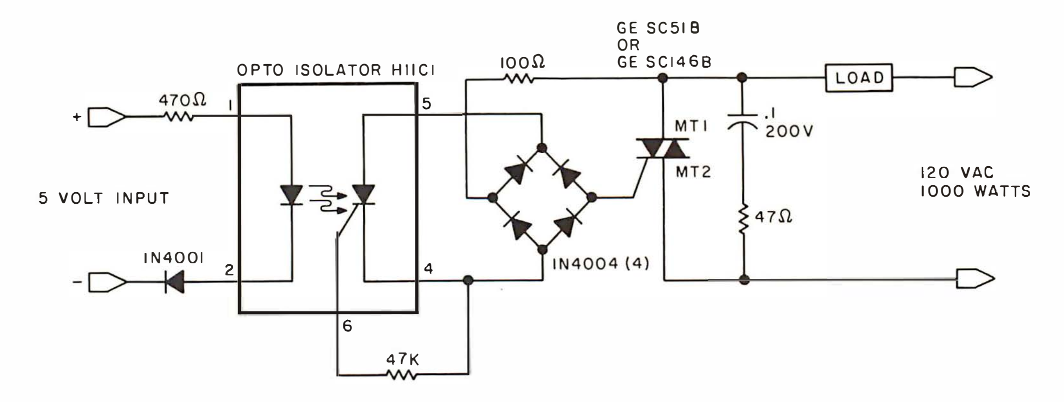


Figure 4: 10 A solid state relay suitable for use in a TTL to 115 VAC application.

works for both set and reset frequencies simultaneously. This same procedure is repeated for any other channel.

Using the System in the Home

The transmitter is plugged into any 110 VAC outlet in the vicinity of the computer.

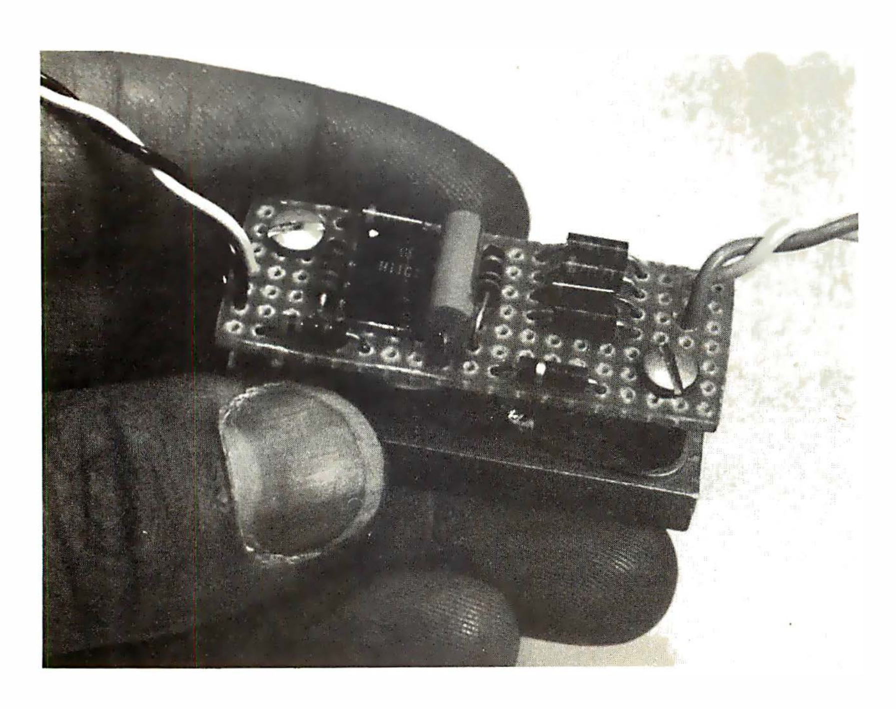


Photo 3: Homemade solid state relay (see figure 4).

```
100   PRINT "WHAT IS THE OUTPUT PORT NUMBER OF THE TRANSMITTER"
110   INPUT N :REM N IS IN DECIMAL
120   PRINT "OUTPUT UPDATE VALUE"
130   INPUT X
140   OUTPUT N, X :REM X is sent to the transmitter DAC
150   GOTO 120
```

Listing 1: A simple BASIC program to aid the user in calibrating the transmitter. A frequency counter is attached to pin 6 of IC3 in the transmitter in order to check the actual output frequency versus a typed in value.

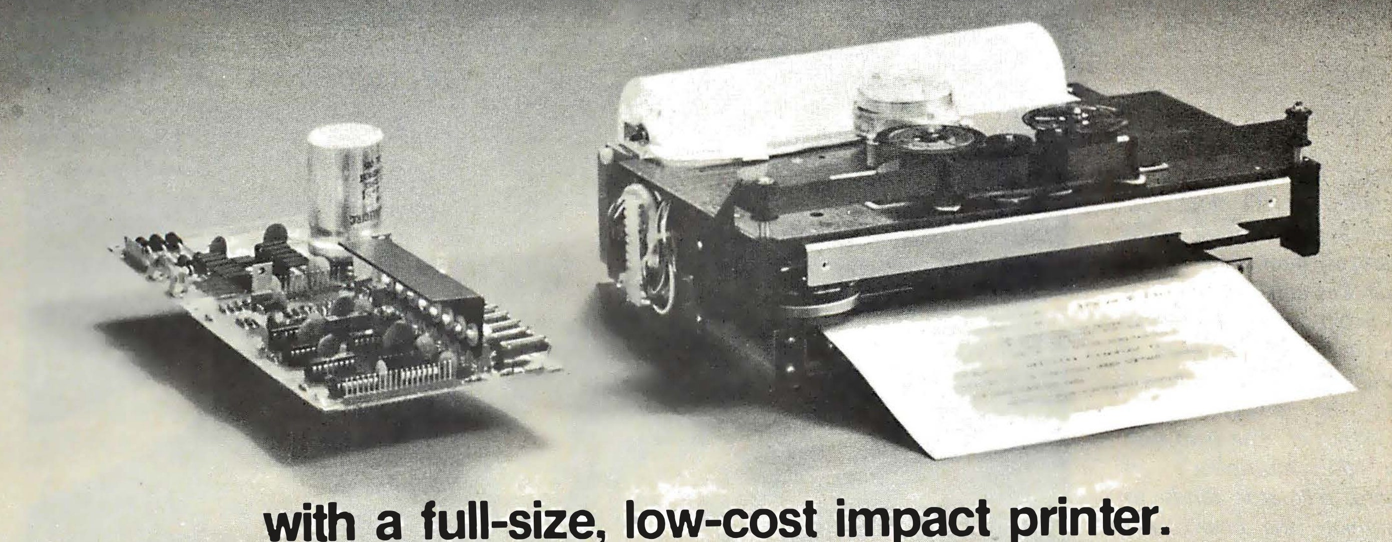
Depending on the home, it may or may not transmit to all outlets in the house. Most homes have 220 V service which consists of two independent 110 VAC lines. A frequency transmitted into one line may not pass over into the other line with sufficient power to be detected at all receiver locations. It may be necessary to take one of the receivers and plug it into a number of different outlets to determine which are on the correct circuit. This potential problem is not unique with this particular design and is a factor to be considered in all carrier current designs. In most cases, if there are sufficient 220 VAC loads in use, such as heaters and stoves, etc, the carrier frequency will pass easily through the loads from one line to the other and the whole house will be covered.

The most obvious application of such a computer control system is a home lighting system used in conjunction with a burglar alarm. The major problem with conventional timer activated light controllers is that their consistently repeated on and off periods are an immediate tip-off that no one is home. With this system and either a real time, time of day clock, or timing loop functioning as a clock, the on and off periods of a number of lights can be altered dynamically. The program which accomplishes this function can be implemented as easily in BASIC as any of the test programs used to check out the AC remote controller described in this article.

I hope that you have enjoyed this latest project and the humorous as well as utilitarian applications of such a system. I'll try to bring you similar projects in the future. If you have questions or comments please feel free to write me and enclose a stamped, self-addressed envelope.

Next month: digitized speech.■

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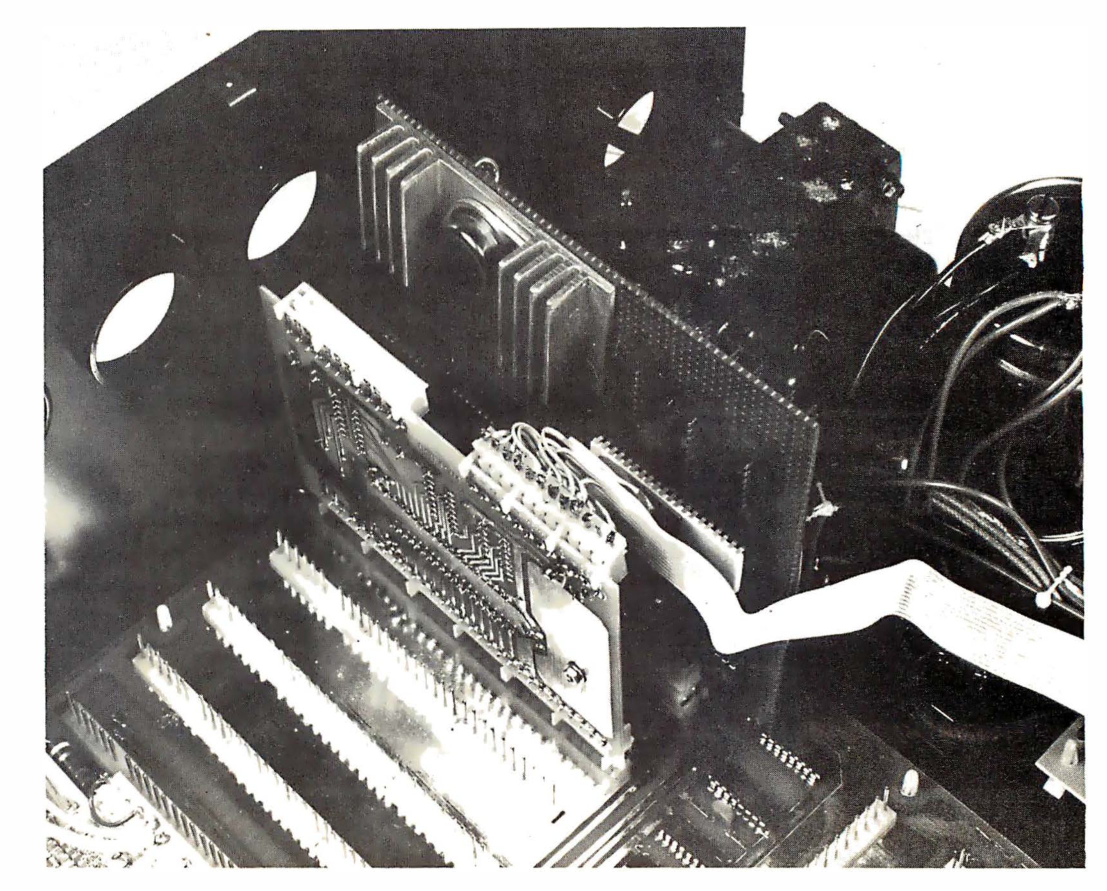


Photo 1: The multiplier installed in IO slot 7 of the SwTPC 6800 processor system. The multiplier was constructed on a perforated board base, and is seen here between a parallel interface board and the power supply transformer. The heat sink for the multiplier's on board regulator tends to dominate the board, and the multiplier integrated circuit itself is the white 40 pin package partially hidden by a cable.

How to Multiply in a Wet Climate

Part 2: Design Details

Jack Bryant
Mathematics Dept
Texas A&M University
College Station TX 77843

Manot Swasdee
E E Dept
Texas A&M University
College Station TX 77843

In last month's article, we discussed microprocessor arithmetic and how an 8 by 8 bit two's complement multiplier could do it faster. Specific examples, in Motorola M6800 assembly language, showed how multiple precision arithmetic and quick matrix addressing could use hardware multiplication. We gave a logical block diagram of a circuit which would make the product (formed by a multiplier array) much easier to use. This month's article contains details needed to construct and fully test a hardware multiplier for the SwTPC 6800 system using the TRW MPY-8AJ and eleven SSI and MSI TTL chips.

This month we give detailed construction information on how to build a wire wrap version of the hardware multiplier for the SwTPC 6800 system. Photo 1 shows the multiplier installed in port 7 of the 6800, which is the object of this effort. We used port 7 because the wire wrap pins would be easily accessible there and would not interfere with other IO interfaces. We begin with some details about the SwTPC mother board address decoding.

Addresses in the 6800 are 16 bits, numbered from most significant to least significant bit as A15, A14 . . . A1 A0. Decoding circuitry on the mother board traps any address starting with binary 100 (ie: with

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Now on CP/M

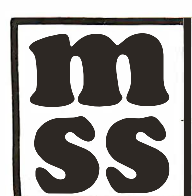
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DS,DV,DP	Diablo Hy-Term	SOL/Cuter,VDM-1/Tarbell,VTI/Tarbell	$150.
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Hexadecimal Address	What Happens When the Computer Writes into this Location		What Happens When the Computer Reads Data from this Location
801C	Clock the multiplicand into MPY-8AJ register X.	Unshifted Product	For the last strobed product, read the left justified high order part of the products: PS, P1, . . ., P7.
801D	Clock the multiplier into MPY-8AJ register Y and strobe the product into product register P.	Unshifted Product	For the last strobed product, read the left justified low order part of the product, with zero for the least significant bit: P8, P9, . . ., P14, 0.
801E	Set control code: binary **** *SFR F = strip sign X S = strip sign Y R = set ROUND * = "don't care"	Right Shifted Product with OV	For the last strobed product, read the overflow bit OV, then right justified and shifted product bits: OV, PS, . . ., P6.
801F	Not used	Right Shifted Product with OV	For the last strobed product, read the right justified and shifted product bits: P7, . . ., P14.
Note: Using terminology of the MYP-8AJ and the previous article of this series, bits of the multiplication data are numbered 0 to 15, most significant to least significant.			
Program Sequence: Set up control code (801E). Store X multiplicand (801C). Store Y multiplicand (801D). Read and use shifted (801E or 801F) or unshifted (801C or 801D) product bytes.			

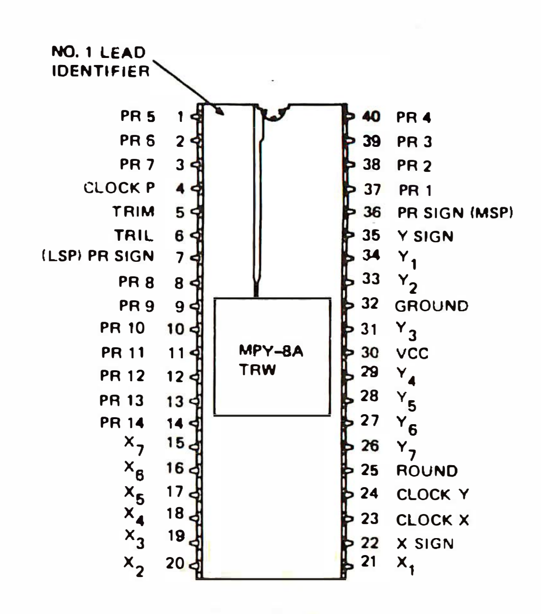
Table 1: Port 7 addresses and significance. Note that writing to the first three addresses is used to control the multiplication: address 801E receives a control code, 801C receives the X operand, and address 801D receives the Y operand and simultaneously forms the product and clocks it into the output register P.

A15=1, A14=0, and A13=0, hexadecimal addresses 8XXX or 9XXX where X means "don't care." The last six bits (A5, A4, A3, A2, A1, and A0) are examined to decode ports. For the first eight slots (one full mother board), A5=0, and bits A4, A3, and A2 are decoded with a 74LS138 3 to 8 line decoder. This signal is port bus pin 1: IO select. Remaining bits A1 and A0 are buffered and become port bus signal RS1 and RS0, used by hardware plugged in a slot to select which of the four bytes is being addressed. (Actually, we earlier used the term "port" rather loosely to mean IO slot. We now wish to be more precise and recognize that each IO slot contains four ports.)

Although the IO slot is only four bytes wide, the bytes which are read need not be logically the same as (or even related to) the bytes which are written to the same address. (Compare this with a memory where we would hope they are the same!) Port bus signal RW tells hardware in an IO slot what to expect. To use our hardware multiplier, we write (from the processor) into three bytes, and read from four bytes of IO slot #7. This is summarized in table 1.

In table 1, the MPY-8AJ registers X, Y and P are mentioned (along with ROUND). Figure 1 is a pinout drawing of the TRW product (reproduced from the specifications sheets, courtesy of TRW Electronics Sys-

Figure 1: Physical layout and pinout diagram for the MPY-8AJ multiplier part, reproduced from the specifications sheets, courtesy of TRW Electronic Systems Division, One Space Park, Redondo Beach CA 90278. Note that bits are numbered from 1 (most significant) to n (least significant), a convention which differs from conventional microprocessor usage in which bit 0 is always the least significant. The text and figures of these articles reflect the inverse ordering of the bit numbers on the multiplier side of the interface.



SCELBI's new '8080' STANDARD ASSEMBLER

FUNCTION: Assembles programs written in symbolic language for an 8080 CPU on an 8080 based system.

HARDWARE REQUIRED: 8080 computer with minimum of 4K memory (of which at least 1K should be RAM); a source listing input device; an object code output device.

OPTIONAL HARDWARE: A system console device such as a keyboard/CRT or keyboard/printer will allow convenient control of the program using executive commands; additional memory beyond 4K will allow expanded symbol table length, or capability to assemble directly into memory.

SOFTWARE REQUIRED: User provided I/O driver routines for whatever I/O devices will be utilized. Each I/O device is linked to the program by a *single* vector for ease in adapting the program to individual systems.

MEMORY UTILIZED: The assembled listing provided in the manual resides in pages 01 through 0A (hexadecimal – 001 through 012 octal). Pages 00, part of 0A, all of 0B and 0C (hexadecimal – 000, part of 012, 013 and 014 octal) are left available for user provided I/O routines. Pages 0D (hexadecimal – 015 octal) on up used for symbol table storage (or as direct assembly areas in systems with sufficient memory).

MNEMONICS UTILIZED: This program is written in, and accepts for assembly purposes, standard industry accepted mnemonics for the 8080 CPU (such as MOV A,B; INX H: CALL; etc.) [Note: SCELBI is discontinuing its use of special 8008 compatible mnemonics which have characterized its 8080 programs in the past.]

PSEUDO-OPERATORS: Accepts the ORG (originate), END (stop assembly), SET (define a name), DB (data byte), DS (data string) and DW (data word or double byte) pseudo-operators.

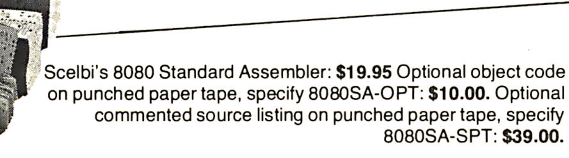
PROGRAM OPERATION: The program processes a source listing in two passes to produce assembled object code. An optional third pass allows an assembled listing to be obtained. Listings may be obtained in hexadecimal or octal format. The program will also display the contents of the symbol table at the operators request. The program can process source listings as single or multiple files. Program operation may be controlled from a console device using executive commands or through computer panel switches by jumping to appropriate locations within the program.

SOURCE FORMAT: Convenient, easy to use, variable length fields permitted. Labels may be 1 to 6 characters in length, accepts both hexadecimal and octal numbers with or without leading zeros, has "literal" capability (can accept ASCII characters directly as data), allows use of letters of numbers as CPU register operands.

DOCUMENTATION: Thorough – in the SCELBI tradition! The program manual describes the operation of the assembler, presents detailed discussions of all major routines, and contains two completely assembled listings (one provided in hexadecimal and one in octal notation). Of course it includes operating instructions and even provides a routine that may be used for loading programs produced by the assembler!

SPECIAL FEATURES: Because the program has been carefully organized and written with all memory references assigned labels, it may be readily reassembled to reside in any general area in memory. It may even be reassembled to reside in ROM provided that some RAM area is available for scratch pad and symbol table use!

OPTIONS: A punched paper tape of the object code for this assembler (as described in the documentation) is available. The object code tape is provided in the widely accepted "hexadecimal format." Also, the complete, commented source listing of the program as presented in the documentation is available in straight ASCII format on punched paper tape. Fan-fold paper tapes are provided for ease in handling. Additionally, opaque paper tape is supplied to facilitate the use of low cost optical paper tape readers now in widespread use. NOTE: Paper tapes are sold only as optional supplements to the documentation.



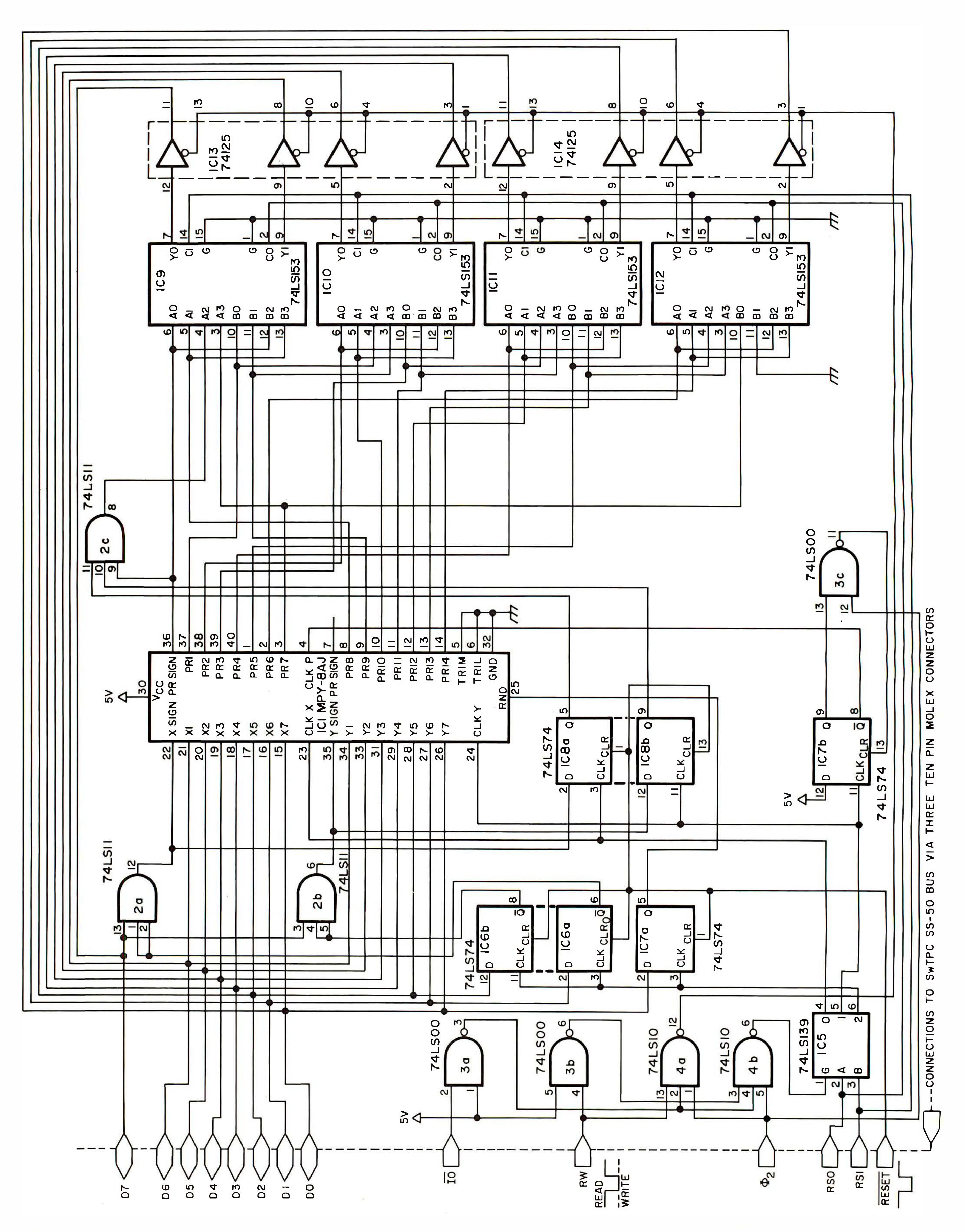
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Figure 2.


IC13 74125
IC14 74125
IC9 74LS153
IC10 74LS153
IC11 74LS153
IC12 74LS153
ICI MPY-8AJ
IC8a 74LS74
IC8b
IC7b 74LS74
IC6b 74LS74
IC6a
IC7a 74LS74
IC5 74LS139
74LS11
74LS00
74LS10
CONNECTIONS TO SwTPC SS-50 BUS VIA THREE TEN PIN MOLEX CONNECTORS
D7
D6
D5
D4
D3
D2
D1
D0
RW
READ
WRITE
RS0
RS1
RESET
5V

POWER WIRING TABLE			
IC Number	Type	+5 V Pin	Gnd Pin
1	MPY-8AJ	30	32
2	74LS11	14	7
3	74LS00	14	7
4	74LS10	14	7
5	74LS139	16	8
6	74LS74	14	7
7	74LS74	14	7
8	74LS74	14	7
9	74LS153	16	8
10	74LS153	16	8
11	74LS153	16	8
12	74LS153	16	8
13	74125	14	7
14	74125	14	7

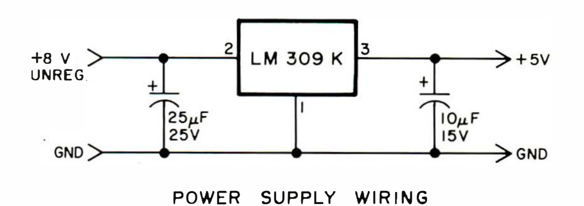


Figure 2: The complete MPY-8AJ multiplier interface. The SwTPC (SS-50) and Motorola symbolic designations of processor signals are shown at the left side of the diagram. RS0 and RS1 are signals derived from the low order address bits A0 and A1 from the processor. IO select is a signal from the SwTPC processor that indicates a reference to a range of four addresses; for slot 7 of the backplane these addresses are 801C and 801F.

tems Division), the basic component of our multiplier. Labelling bits as TRW does, from 1 (most significant) to 14 (least significant), we can write:

$$X = -x_s + x_1 2^{-1} + \ldots + x_7 2^{-7},$$

$$Y = -y_s + y_1 2^{-1} + \ldots + y_7 2^{-7}; \text{ then}$$

$$P = X * Y = -p_s + p_1 2^{-1} + \ldots + p_{14} 2^{-14} + \text{ROUND} \cdot 2^{-8}.$$

Signals CLOCK X and CLOCK Y move X and Y from the data bus to the multiplier array input registers. In our application, we treat sign bits x_s and y_s differently: these are data bus signals ANDed with a control code bit which is stored in a flip flop and used to control stripping of signs.

The MPY-8AJ pinout suggests an intention of the designers to use the upper and lower parts of the product independently. In fact pin 5, called TRIM, enables the three state output buffer for the most significant part of the product ($p_s\ p_1 \ldots p_7$), and pin 6 labelled TRIL enables the least significant $p_s\ p_8 \ldots p_{14}$. However, we are treating the product here as a single 15 bit entity (which we optionally return shifted left or right), and do not require the TRIL and TRIM signals since external logic is employed in the circuit.

In our design the CLOCK P signed is generated 1/2 clock cycle after the storing in (writing to) the Y register at hexadecimal address 801D. We could have used some other signal to clock the product into output registers, but this would usually take another instruction. Usage of the multiplier can be summarized as follows:

1. Set condition (which is set to 0 by RESET).
2. Store multiplicand X.
3. Store multiplier Y.
4. Read product as needed.

The third and fourth steps may be repeated (for as many distinct multipliers as are needed) without storing another X. However, the condition code which prevailed when the last X was stored determines whether the sign of X is stripped. The product remains unchanged until another multiplier is stored in hexadecimal 801D. (The reason for stripping signs was explained last month.)

One product of signed 8 bit numbers treated as fractions seems "wrong": $-1 \times -1 = -1$. Recall that -1 is equal to the binary value 1000 0000; there is simply no representation of +1 as a signal binary fraction. (Thinking of the same binary numbers as integers with the binary point to the right leads to a different interpretation: there is no 15 bit two's complement representation of decimal 16,384 = 2^{14}. That is, the product of -128 times -128 exceeds the capacity of 14 bits.) Actually, the product is correct "modulo 2." In any case, it represents an overflow condition which needs to be flagged if possible, mainly because it is so hard to detect with software. Luckily, with this design we have a spare bit

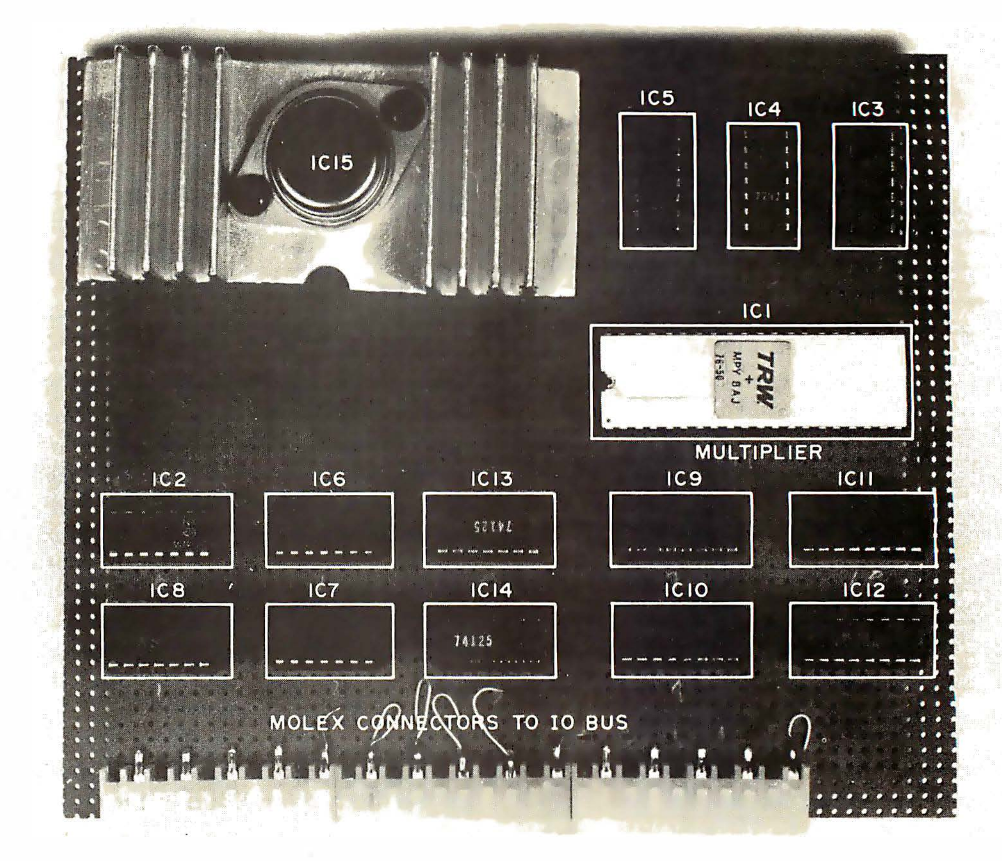


Photo 2a: Component side of the multiplier board. The circuit is entirely socketed with wire wrap sockets. The Molex connectors are mounted on the component side, with every other pin connection made by running wire wrap to solder terminations on the component side. The overlay shows logical identifications of components from figure 2.

in a good place. The first bit of hexadecimal location 801D (which is usually 0). We turn this bit on when the product of two negative numbers turns out to be negative.

How to Build the Multiplier

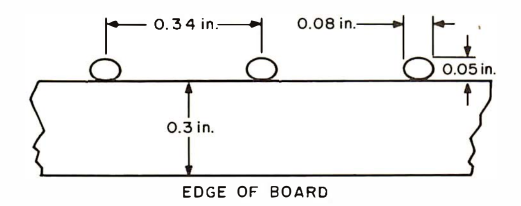
Figure 2 is a circuit diagram of the hardware multiplier. The prototype discussed here was built in a few hours using the nifty OK Machine & Tool Corporation WSU-30 hand wire wrap tool ($5.95 from James Electronics and others).

Wire wrap DIP sockets are inserted into prepunched .1 inch grid Vectorboard. The layout of the integrated circuits is shown by the overlay on photo 2a. Molex sockets are used to plug into SwTPC IO ports; three 10 pin connectors are needed. Since Molex connectors are not spaced on the .1 inch grid of the Vectorboard, slots must be cut in the Vectorboard to accommodate and hold the connectors. Figure 3 shows the dimensions of the slots and their placement on the Vectorboard. Such slots can be made most easily with a Dremel tool equipped with the tiny router type tip. The width of the slots is important: if the slots are too wide, it will be hard to get a solid mounting.

After all slots are cut, insert the connectors with the plastic hooks catching the edge of the Vectorboard. Gently push the solder tabs into the slots, pushing the connector against the Vectorboard while bending the extended solder tab toward the edge of the board (see photo 2b). Wires may now be soldered to solder tabs and brought to the proper wire wrap socket. We got a good mounting with every other pin straightened out (so that only half as many slots need be cut).

No unexpected surprises accompany wire wrapping the circuit, although the WSU-30 requires a little practice before good tight wraps are obtained.

Figure 3: Size and spacing of Molex connector slots relative to lower board edge.



Note: The MPY-8AJ is available in single unit quantities from TRW, One Space Park, Redondo Beach CA 90278. The authors have a few on hand for $100 postpaid.

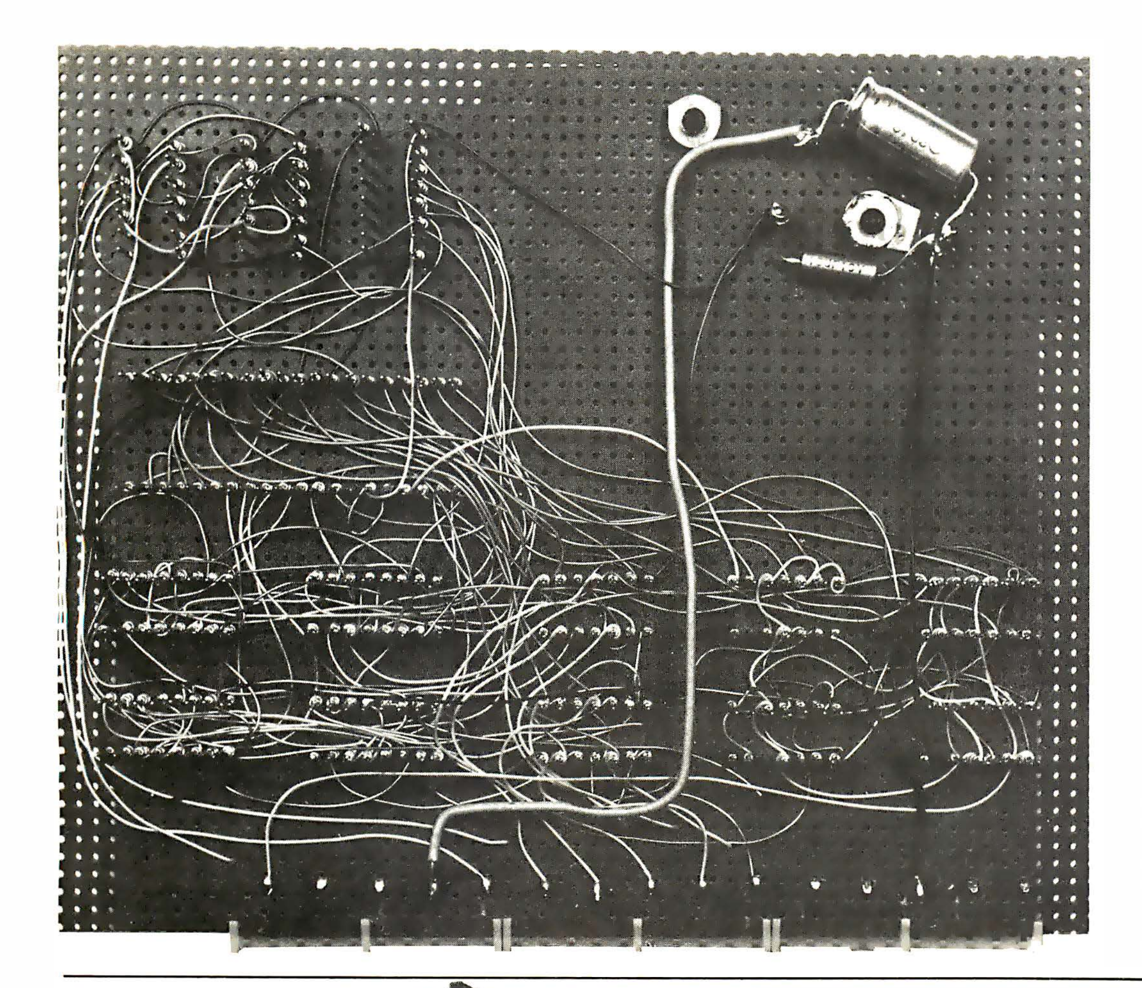


Photo 2b: The wiring side of the wire wrap prototype of the high speed multiplier. The Molex pins are bent over for mechanical support. All connections are wire wrapped with the exception of capacitors in the power supply and terminations to the Molex connector.

Table 2: A list of SwTPC 6800 computer system IO bus pins and calculated worst case loading of these pins by the circuit of figure 2. The worst case loading is the current drawn when an input is in the logical 0 state. (The 0.5 A power supply loading into the regulator is not a logic signal, of course, and the GND pins have no such specification applicable.)

Pin	Signal	Worst Cast Zero Level Load	Pin	Signal	Worst Case Zero Level Load
1	IO #	−0.36 mA	16	D3	−0.42 mA
2	RESET	−3.60 mA	17	D2	−1.16 mA
3	110 b	NC	18	D1	−1.16 mA
4	150 b	NC	19	D0	−1.16 mA
5	300 b	NC	20	RS1	−1.80 mA
6	600 b	NC	21	RS0	−1.18 mA
7	1200 b	NC	22	IRQ	NC
8	+8 unreg	500 mA	23	NMI	NC
9	+8 unreg		24	INDEX	NC
10	R/W	−0.72 mA	25	GND	GND
11	φ2	−1.08 mA	26	GND	GND
12	D7	−0.72 mA	27	+12	NC
13	D6	−0.42 mA	28	−12	NC
14	D5	−0.42 mA	29	UD4	NC
15	D4	−0.42 mA	30	UD3	NC

Listing 1: Support software and test program for the hardware multiplier. This listing gives the complete source code and assembly listing of a 6800 processor program which tests the operation of the multiplier circuit in a SwTPC 6800 computer system. The operation of the hardware multiplier is compared to an implementation of a version of Booth's algorithm for signed two's complement multiplication. IO operations are performed with Motorola MIKBUG subroutines.

```
*   PROGRAM TESTMP
*
*   PURPOSE:  TO TEST A HARDWARE MULTIPLIER
*       DESIGNED FOR THE  SWTP  M6800 SYSTEM
*       USING A  TRW  MPY-8AJ TWOS COMPLEMENT
*       ASYCHRONOUS PARALLEL MULTIPLIER.
*
*   DESIGN:
*       HARDWARE:  MANOT SWASDEE
*       SOFTWARE:  JACK   BRYANT
*
*   PARAMETERS:
*
*       FOR SUBROUTINE BOOTH8:
*
*       M -- ONE OPERAND FOR SOFTWARE MULTIPLIER
*       R -- OTHER OPERAND
*       P -- TWO BYTE PRODUCT.
*
*       FOR HARDWARE MULTIPLIER:
*
*                   INPUT              OUTPUT
*                   =====              ======
*     FM -- FIRST OPERAND       SIGN AND UPPER
*                               7 BITS OF PRODUCT
*
*     SM -- SECOND OPERAND      LOWER 7 BITS
*           & STROBE PRODUCT      AND ZERO
*
*    URP -- CONDITION CODE:     BIT 0: OVERFLOW
*           XXXXXSFR WHERE      (ON $80*$80)
*         F = STRIP SIGN FM     BITS 1-7: SIGN
*         S = STRIP SIGN SM     AND UPPER 6 BITS
*         R = ROUND             OF PRODUCT
*         X = DON'T CARE
*
*    LRP -- NOT USED FOR        LOWER 8 BITS
*           INPUT               OF PRODUCT
*
*   USAGE:
*       THIS PROGRAM ASSUMES THE HARDWARE
*       MULTIPLIER IS CONFIGURED AT ADDRESS
*       $801C-$801F. WHICH IS PORT 7 IN THE
*       SWTP 6800 SYSTEM.  FOR ANOTHER, CHANGE
*       FM        EQU      $801C
*       TO THE DESIRED ADDRESS.
*       FAILURE DURING TEST RESULTS IN THE
*       EXECUTION OF A  SWI  INSTRUCTION.
*       RETURNING CONTROL TO  MIKBUG
*       OPERATING SYSTEM.  CURRENT VALUES
*       OF PARAMETERS CAN BE FOUND USING THE
*       MEMORY EXAMINE AND CHANGE FUNCTION.
*
*         OPERAND              ADDRESS
*       FIRST MULT.             $0004
*       SECOND MULT.            $0005
*       CONDITION               $0006
```

How to Test It: Booth's Algorithm

Listing 1 is a program which repeatedly tests every function of the hardware multiplier with every possible combination of operands and condition code against a software generated product. For each of eight values of the condition code, all 65,536 different products are formed and compared. This is a lot of logic and arithmetic, and we sought a more efficient software multiply method than program MPY8S0 in listing 3 of the first part of this article. Such an algorithm was discovered in 1951 by Andrew Booth; this was quickly coded up and tested. (Surprise: in Booth's notation, the algorithm fails on the expression m x r if r = −1, although it does evaluate −1 x r correctly. The reason is that there is no two's complement of −1. That is, this two's complement value overflows and the algorithm gets started incorrectly. The result is m x −1 = m, which is only correct if m equals 0 or −1. Booth's "proof" really shows only that m x r is correct when r is regarded modulo 2; since −1 and 1 are the same modulo 2, in some sense the algorithm works. In any case, an inelegant fix is to interchange m and r if r = −1.)

Algorithm 1 shows what the test program does, and algorithm 2 is (our modification of) Booth's algorithm. The test program rings the system bell (ASCII 07) every time the condition code changes, with every eighth bell ring being replaced by a print of "OK." Each complete cycle takes a little over 3 1/2 minutes, with about 42 seconds separating bell rings. (Booth's algorithm is about twice as fast as MYP8S0, although it is trickier. We get about 1560 tests per second [most of this time is spent in BOOTH8] or about 641 μs per test.)

Bus Loading

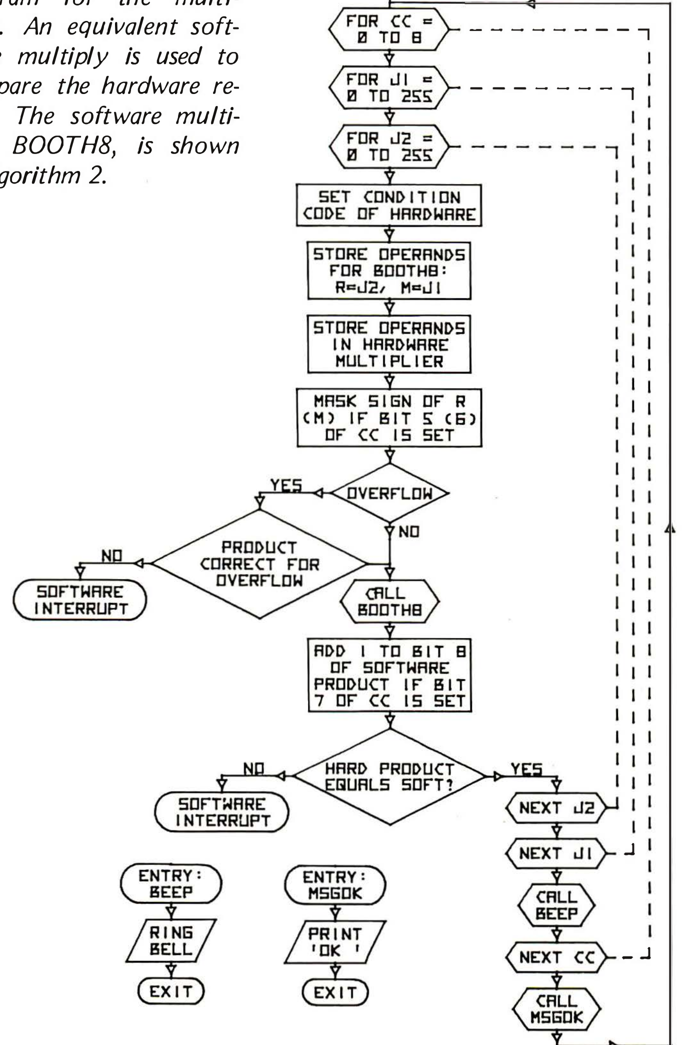
One point we have neglected is the problem of how heavily we are loading the system bus. In order to allow the seven other slots to be full of IO interfaces or other loads, we indicate use of 74LS series TTL. The worst case loading is shown in table 2. The MPY-8AJ input loading is less than 1 mA without input buffering. Table 2 also gives SwTPC bus pin number identifications.

REFERENCE

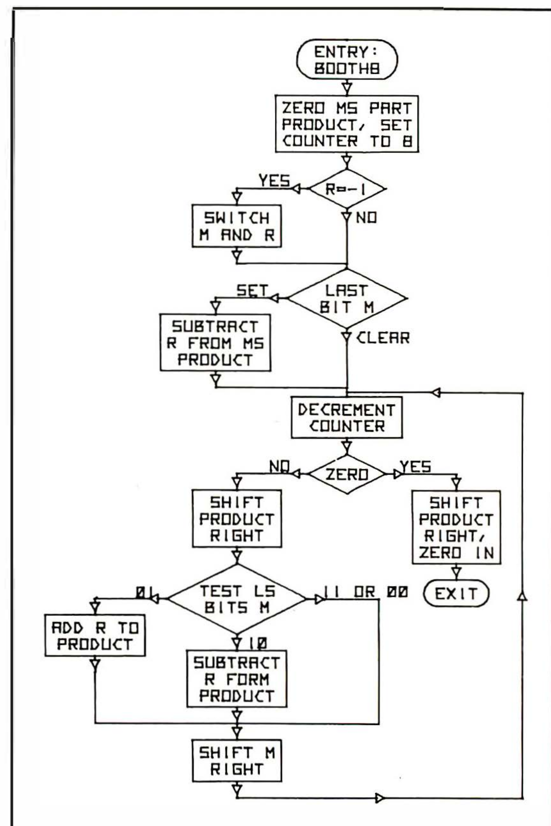
Andrew D Booth, "A Signed Binary Multiplication Technique," *Quarterly Journal of Mechanics and Applied Mathematics,* volume 4 (1951), pages 236 to 240. Reprinted in *Computer Design and Development: Principal Papers,* edited by Earl E Swartzlander Jr, Hayden Book Company, Rochelle Park NJ, 1976, pages 163 to 166.

Listing 1, continued:

```
                      *
                      *      SUCCESS OF TEST IS INDICATED BY
                      *      PERIODIC RINGING OF THE BELL AND
                      *      OUTPUT OF THE MESSAGE 'OK ' EVERY
                      *      COMPLETE CYCLING.  TO STOP THE TEST,
                      *      PRESS 'RESET'.
                      *
                      *      EACH CYCLE OF THE TEST TAKES ABOUT
                      *      FIVE MINUTES, THIRTY SECONDS, WITH
                      *      THE BELL RINGING EVERY 42 SECONDS.
                      *
           E1D1       OUTEEE EQU    $E1D1    MIKBUG OUTPUT SUBROUTINE
           801C       FM     EQU    $801C
           801D       SM     EQU    FM+1     PORT 7
           801E       URP    EQU    FM+2     VIA SWTP.
           801F       LRP    EQU    FM+3
     0000  0001       M      RMB    1        FIRST MULT. FOR BOOTH8
     0001  0001       R      RMB    1        SECOND MULT.
     0002  0002       P      RMB    2        PRODUCT.
     0004  0001       J1     RMB    1        'RAW' FIRST MULT.
     0005  0001       J2     RMB    1        'RAW' SECOND MULT.
     0006  0001       CC     RMB    1        CONDITION.
     0007  7F  C0C6   AGAIN  CLR    CC
     000A  7F  C0C4   NEXTCC CLR    J1
     000D  7F  0005   NEXTJ1 CLR    J2
     0010  96  C6     NEXTJ2 LDA A  CC       SET CONDITION CODE
     0012  B7  801E          STA A  URP      OF HARDWARE.
     0015  96  C4            LDA A  J1       STORE FIRST
     0017  B7  801C          STA A  FM       MULTIPLICAND.
     001A  97  00            STA A  M        SAVE FOR BOOTH8.
     001C  96  C5            LDA A  J2       SAME FOR
     001E  B7  801D          STA A  SM       MULTIPLIER.
     0021  97  01            STA A  R        SAVE FOR BOOTH8.
                      *
```



Algorithm 1: A test program for the multiplier. An equivalent software multiply is used to compare the hardware result. The software multiply, BOOTH8, is shown in algorithm 2.



Algorithm 2: BOOTH8, a faster 8 bit by 8 bit multiplication algorithm which replaces listing 3 of part 1 of this article in order to speed up tests of the multiplier circuit. As in part 1 of this article, the author's original flowchart representations which were drawn with a computer controlled plotter are reproduced here.

Listing 1, continued:

```
0023 96 C6            LDA A  CC        IS BIT 5 OF CC SET?
0025 84 04            AND A  #4
0027 27 C6            BEQ    NOT5
0029 96 C1            LDA A  R         YES.
002B 84 7F            AND A  #$7F      MASK SIGN OF R.
002D 97 01            STA A  R
                *
002F 96 C6      NOT5  LDA A  CC        IS BIT 6 OF CC SET?
0031 84 02            AND A  #2
0033 27 C6            BEQ    NOT6
0035 96 00            LDA A  M         YES.
0037 84 7F            AND A  #$7F      MASK SIGN OF M.
0039 97 C0            STA A  M
                *
003B 86 80      NOT6  LDA A  #$80      SEE IF $80*$80.
003D 91 00            CMP A  M
003F 26 14            BNE    NOOVFL
0041 91 01            CMP A  R
0043 26 10            BNE    NOOVFL
0045 B6 E01E          LDA A  URP       OVERFLOW HERE.
0048 81 C0            CMP A  #$C0      SEE IF URP=%1100 0000
004A 27 47            BEQ    BUMPJ2
004C 3F               SWI              ERROR IN FORMING
                *                        OVERFLOW BIT.
                *
004D 20 BB      NEXCC  BRA   NEXTCC    BRIDGE FOR
004F 20 BF      NEXJ2  BRA   NEXTJ2    LONG JUMPS
0051 20 EA      NEXJ1  BRA   NEXTJ1    FOR RELATIVE
0053 20 E2      AGN    BRA   AGAIN     BRANCHING.
                *
0055 BD 00C4    NOOVFL JSR   BOOTH8    FORM SOFTWARE PROD.
0058 96 C6            LDA A  CC
                *
005A 84 C1            AND A  #1        ROUND?
005C 27 0F            BEQ    NOCARY
005E 96 03            LDA A  P+1       YES.  ADD 1
0060 8B 40            ADD A  #$40      TO BIT 8 OF
0062 97 03            STA A  P+1       PRODUCT, WHICH
0064 24 C7            BCC    NOCARY    IS BIT 1 OF P+1
0066 96 02            LDA A  P
0068 4C               INC A            TURN BIT 0 BACK OFF
0069 84 7F            AND A  #$7F
006B 97 C2            STA A  P
                *
006D B6 E01F    NOCARY LDA A  LRP      CHECK LRP.
0070 91 03            CMP A  P+1
0072 27 C1            BEQ    CK1
0074 3F               SWI              ERROR IN LRP.
                *
0075 B6 E01E    CK1   LDA A  URP
0078 91 C2            CMP A  P         CHECK URP.
007A 27 01            BEQ    CK2
007C 3F               SWI              ERROR IN URP.
                *
007D 78 0003    CK2   ASL    P+1       SHIFT PRODUCT
0080 79 C002          ROL    P         LEFT.
0083 B6 E01D          LDA A  SM
0086 91 03            CMP A  P+1       CHECK SM.
0088 27 C1            BEQ    CK3
008A 3F               SWI              ERROR IN SM.
                *
008B B6 E01C    CK3   LDA A  FM
008E 91 02            CMP A  P         CHECK FM.
0090 27 C1            BEQ    BUMPJ2
0092 3F               SWI              ERROR IN FM.
                *
0093 7C C005    BUMPJ2 INC   J2
0096 26 B7            BNE    NEXJ2     INCREMENT J2.
0098 7C C004          INC    J1
009B 26 E4            BNE    NEXJ1     INCREMENT J1
009D 96 C6      BUMPCC LDA A CC
009F 4C               INC A
00A0 81 C8            CMP A  #8        INCREMENT CC.
00A2 27 C6            BEQ    MSG
00A4 97 C6            STA A  CC
00A6 8D C6            BSR    BEEP      RING BELL.
00A8 20 A3            BRA    NEXCC
00AA 8D 08      MSG   BSR    MSGOK     WRITE 'OK '.
00AC 20 A5            BRA    AGN
                *
00AE 86 C7      BEEP  LDA A  #7
00B0 BD E1D1          JSR    OUTEEE
00B3 39               RTS
00B4 86 4F      MSGOK LDA A  #'O
00B6 BD E1D1          JSR    OUTEEE
00B9 86 4B            LDA A  #'K       OUTPUT VIA MIKBUG.
00BB BD E1D1          JSR    OUTEEE
00BE 86 20            LDA A  #$20
00C0 BD E1D1          JSR    OUTEEE
00C3 39               RTS
                *  SUBROUTINE BOOTH8
                *
                *  PURPOSE:  TO PERFORM MULTIPLICATION OF
                *      TWO 8 BIT TWOS COMPLEMENT NUMBERS
                *      GIVING A 14 BIT PLUS SIGN PRODUCT.
                *
                *  METHOD:
                *      BOOTH'S ALGORITHM.
                *
                *  PARAMETERS:
                *      M -- MULTIPLICAND
                *      R -- MULTIPLIER
                *      P -- PRODUCT
                *           0 IN BIT 0
                *           SIGN IN BIT 1
                *           BITS 2-15 HOLD PRODUCT.
                *
                *  RESTRICTIONS:
                *      THE INDEX REGISTER AND BOTH
                *      ACCA AND ACCB ARE DESTROYED.
                *
                *  REFERENCE:
                *      ANDREW D. BOOTH, A SIGNED BINARY
                *      MULTIPLICATION TECHNIQUE, QUART. J.
                *      MECH. APPL. MATH. 4(1951),236-240.
                *
00C4 7F 0002    BOOTH8 CLR   P         ZERO PRODUCT MS
00C7 CE C0C8          LDX    #8        PART.  SET COUNTER.
00CA 07               TPA              SAVE PROCESSOR CONDITION
00CB 36               PSH A            CODES ON STACK.
00CC D6 C1            LDA B  R
00CE C1 80            CMP B  #$80      METHOD HAS A BUG
00D0 26 05            BNE    NOTM1     FOR M*(-1), BUT
00D2 17               TBA              (-1)*R WORKS.
00D3 D6 00            LDA B  M         INTERCHANGE M AND R.
00D5 97 00            STA A  M
00D7 96 C0      NOTM1 LDA A  M         GET STARTED WITH
00D9 06               TAP              BIT 8 ZERO.
                *
                *      THE PROCESSOR CONDITION CODE REGISTER
                *      IS USED TO TEST BITS 6 AND 7:  V IS
                *      BIT 6, C IS BIT 7.
                *
00DA 24 C5            BCC    SHIFT
00DC 96 02            LDA A  P         CASE 10 = SUBTRACT.
00DE 10               SBA
00DF 97 C2            STA A  P
00E1 09         SHIFT DEX
00E2 27 1E            BEQ    FINISH    DECREMENT COUNTER & TEST.
00E4 77 0002          ASR    P         SHIFT PRODUCT RIGHT.
00E7 76 C003          ROR    P+1
00EA 96 C0            LDA A  M
00EC 06               TAP              TEST MULTIPLIER.
00ED 24 C7            BCC    X0
00EF 29 0C            BVS    SHTM
00F1 96 C2            LDA A  P         CASE 01 = ADD.
00F3 1B               ABA
00F4 20 C5            BRA    STAG
00F6 28 C5      X0    BVC    SHTM
00F8 96 C2            LDA A  P         CASE 10 = SUBTRACT.
00FA 10               SBA
00FB 97 C2      STAG  STA A  P
00FD 77 C000    SHTM  ASR    M         SHIFT MULTIPLIER RIGHT.
0100 20 DF            BRA    SHIFT
0102 74 C002    FINISH LSR   P         HERE, PRODUCT IS
                *      LEFT-JUSTIFIED, WITH LEAST SIGNIFICANT
                *      BIT OF P+1 UNDEFINED.  FIX.
                *
0105 76 C003          ROR    P+1
0108 32               PUL A            RESTORE PROCESSOR
0109 06               TAP              CONDITION CODE.
010A 39               RTS
                      END ■
```

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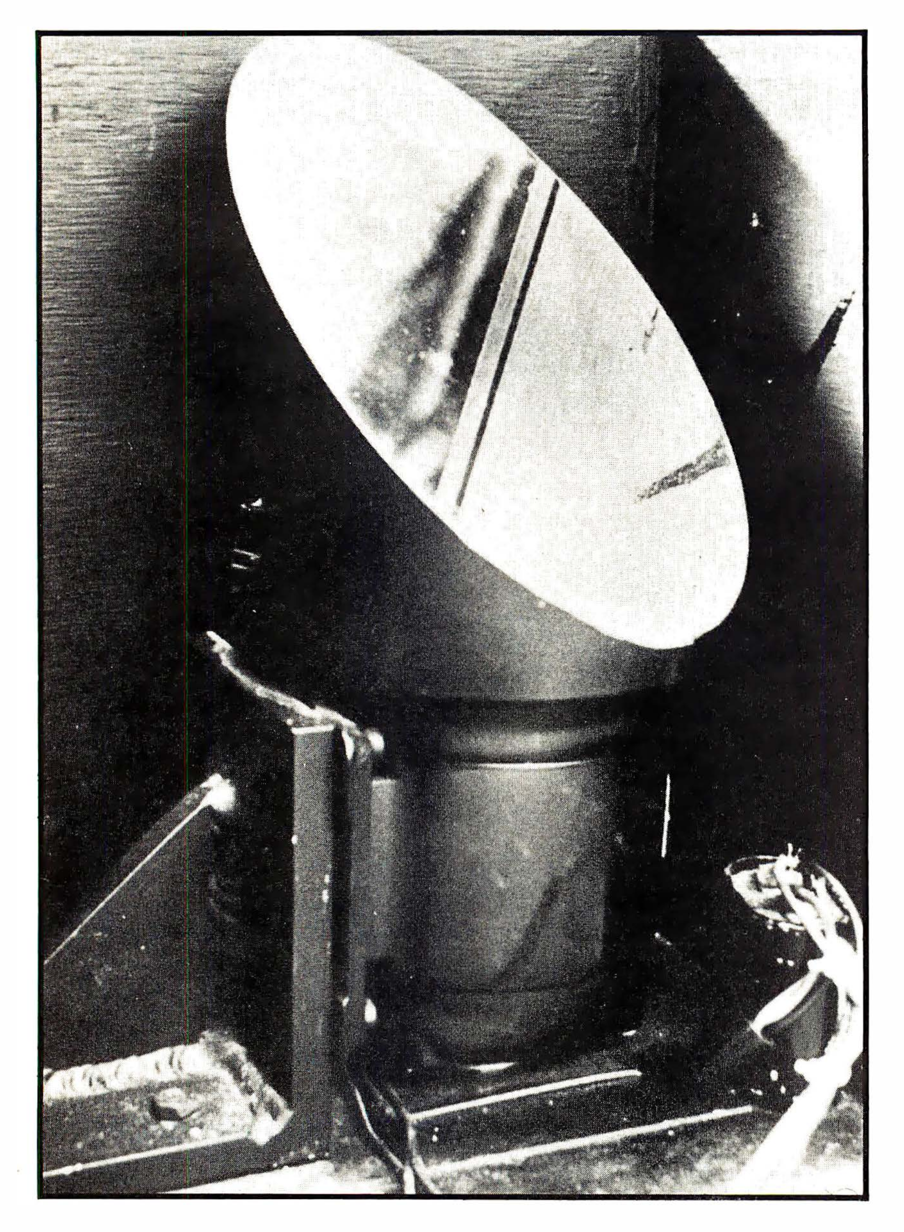


Photo 4: *The original rotating mirror, constructed from milled aluminum.*

Continued from page 18

tional accuracy of 0.01 inches (0.025 cm) in a volume of 3 by 3 by 6 inches (7.6 by 7.6 by 15.2 cm); yet the system uses only a minimal interface to an inexpensive XY oscilloscope display, and the program (written here in MaxiBASIC) can run in as little as 18 K bytes of memory.

A Spinning Mirror

Theoretically, a 3-D display could be built by rapidly moving an oscilloscope display backward and forward in space. At any given moment, the display would be a certain distance from the observer. Any points displayed at this time would appear to be at this depth. Of course, there are mechanical problems involved with this technique. Fortunately, the same effect can be achieved by moving a mirror in front of an oscilloscope screen and viewing the reflection. This technique is illustrated in figure 1. Here a vertical mirror is rotated in front of the screen, causing the reflected image to move in space. Related techniques involving reflected displays are listed in the references.

Once a rotating mirror is built, display of a point in three dimensions becomes a matter of timing and geometry. The vertical mirror is the simplest to build. It is also easy to compute the appropriate geometrical transformations. This design does suffer from a limited field of view, however: the oscilloscope screen itself blocks the display volume somewhat. This type of rotating mirror may be built by mounting a metallic or plastic mirror on the shaft of a motor which can rotate at between 600 to 1200 rpm. A variable speed motor offers some flexibility in the operation of the display. *Note:* For reasons of safety, the reflecting surface of the mirror should be made of either metal or reflective plastic (such as aluminized Mylar). DO NOT use a glass mirror!

An alternate method of construction is shown in photo 4. Here a mirror slanted at a 45° angle is mounted on the shaft of a motor, which is connected to a Variac variable speed motor control. This mirror was built under a National Institute of Health grant. It was milled from a solid block of 6 inch (15 cm) diameter cylindrical aluminum stock. The back of the mirror has been cut away for better dynamic balancing. The

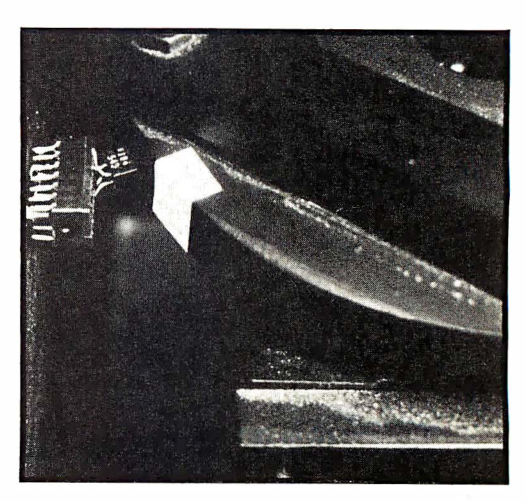
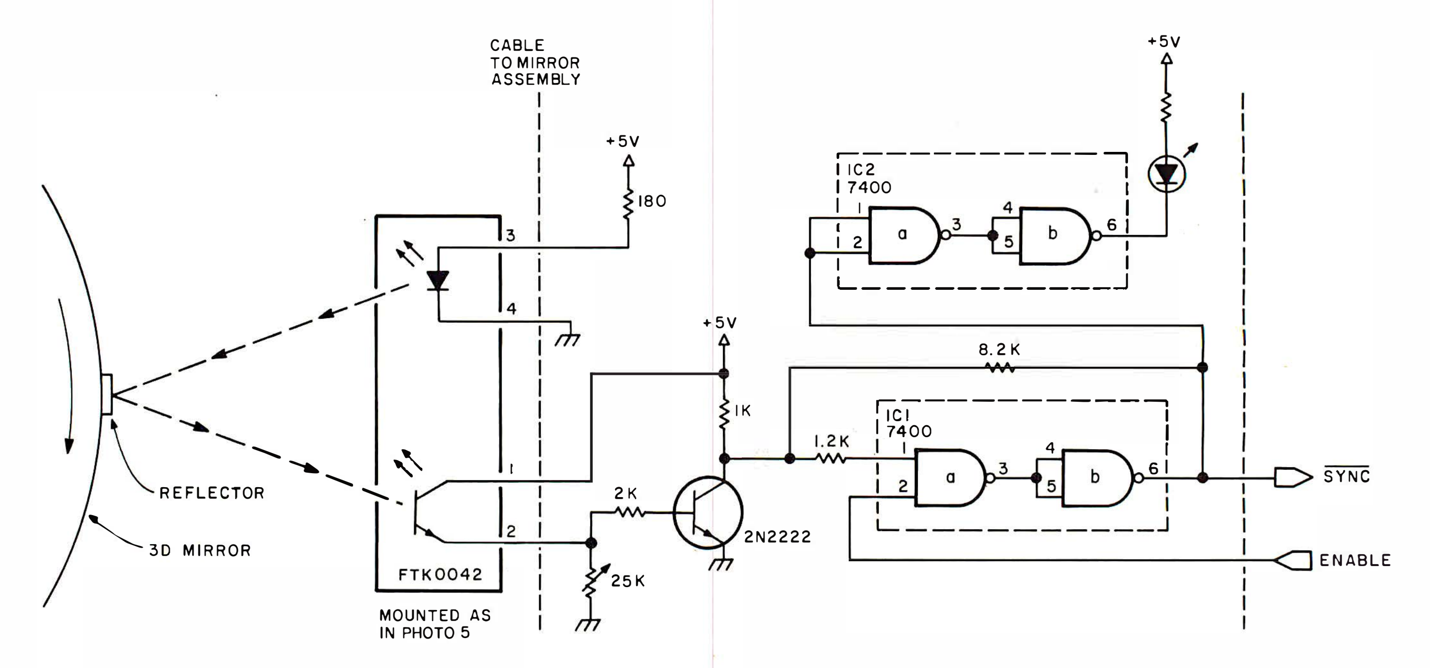


Photo 5: Close-up of the opto-coupler and white timing mark (a piece of tape).

Circle 292 on inquiry card.

Figure 2: Spinning mirror opto-coupler interface. A reflective opto-coupler (photo 5) is used to synchronize the position of the mirror with the program driving the display (photos 2b and 4). The circuit shown converts pulses from the opto-coupler to TTL level signals. Note the use of a feedback resistor at IC1 to form a Schmitt trigger.



mirror and motor are housed in a plywood frame, with all interior surfaces except the mirror face painted flat black to minimize reflections from room lighting.

The display time of a point must be coordinated with the angle of the mirror. This is accomplished with a timing mark on the side of the mirror, consisting of a small piece of white tape which is viewed by a reflective opto-coupler. The opto-coupler is shown in photo 5. The unit consists of a matched phototransistor and light emitting diode (LED) mounted in a single package. The direction of emission and detection is away from the body of the package, so that it can detect the passage of a reflective surface. This system uses a Fairchild Technology Kit FTK0042 coupler. The circuit for converting the light levels to a TTL signal, taken from the documentation supplied with the kit, is shown in figure 2 and consists of a driver transistor connected to the input of a TTL gate. The output of the second inversion stage is connected through a resistor to the input to add enough feedback to form a Schmitt trigger.

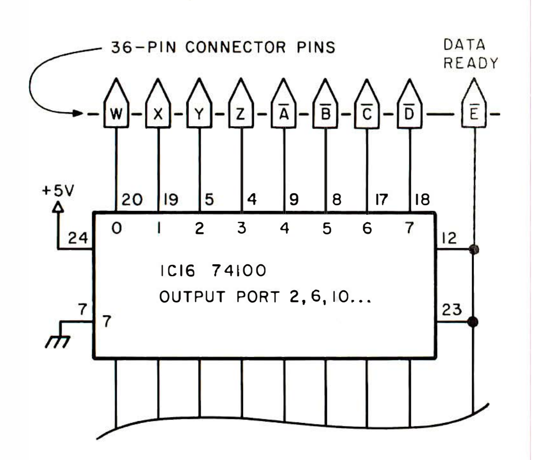


Figure 3: Modification to the Digital Group IO board. The Z-80 processor, which forms the heart of the Digital Group computer, features a block output instruction (OTIR) that can output 1 byte every 9 µs using the standard 2.5 MHz clock. This degree of speed is needed to output the data needed for the 3-D display without using direct memory access circuitry. Adding the data ready line (shown in grey) to IC16 (Digital Group numbering) creates a status signal to the mirror circuitry. This avoids the necessity of using output bits from another port for this purpose, which would slow down the data transfer rate. (The choice of port 2 for the output port is particular to the authors' system.)

Timing and Display of Points

To obtain reasonable persistence in the display, a refresh rate of at least ten frames per second must be maintained. Although this flicker is still observable, it does not seem to be too objectionable. Since the 45° mirror we have been describing reflects the oscilloscope screen during something less than 150° of its rotation, this means that about 40 ms are available to put up all of the display points. Also, since the screen image is continually moving, an accuracy of about 35 µs must be maintained in the timing of the display points to achieve a 0.5% accuracy in the position of each displayed point in a typical image. Obviously, it is necessary to

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Circle 276 on inquiry card.

put up points as quickly as possible to achieve a reasonable density and accuracy in the display. This eliminates standard video displays for the display screen, since the display time of an individual point cannot be controlled to any better than 16 ms on a video display. Instead, it is necessary to use an XY display controlled by digital to analog converters such as the "Beer Budget" graphics interface described in the November 1976 BYTE, page 26. Although any system with a randomly addressable XY display will work, it is desirable to minimize the amount of time required to display each point so that the greatest possible number of points can be displayed.

The Z-80 processor in the Digital Group system has a block output instruction (OTIR) which can output a byte every 9 μs with the standard 2.5 MHz clock rate. This high transfer rate to a pair of 8 bit digital to analog converters gives the lowest possible transfer time without a special direct memory access (DMA) circuit. However, the output from a standard Digital Group parallel IO port consists of just the eight bits of data with no provision for control lines to indicate when the output byte is meant for the X digital to analog converter and when it is meant for the Y digital to analog converter. Using one of the output bits of the port for control would allow only seven bits of resolution, while using output bits from another port for control would require additional IO instructions and would slow down the transfer of data. In order to make use of the high output rate of this instruction, the IO board was modified as shown in figure 3. The write strobe signal for output port 2 was fed to an uncommitted pin on the card to be used as a data ready signal. This was used, along with the port data, as input to a control circuit for the digital to analog converters, as shown in figure 4. The choice of port 2 for the output port is particular to our system. This control circuit is based on the schematic of

Power Connections

IC	Type	+5 V	Gnd
1	74100	24	7
2	74100	24	7
3	MC1408L8	13	2
4	74100	24	7
5	MC1408L8	13	2
6	7430	14	7
7	7476	5	13
8	7400	14	7

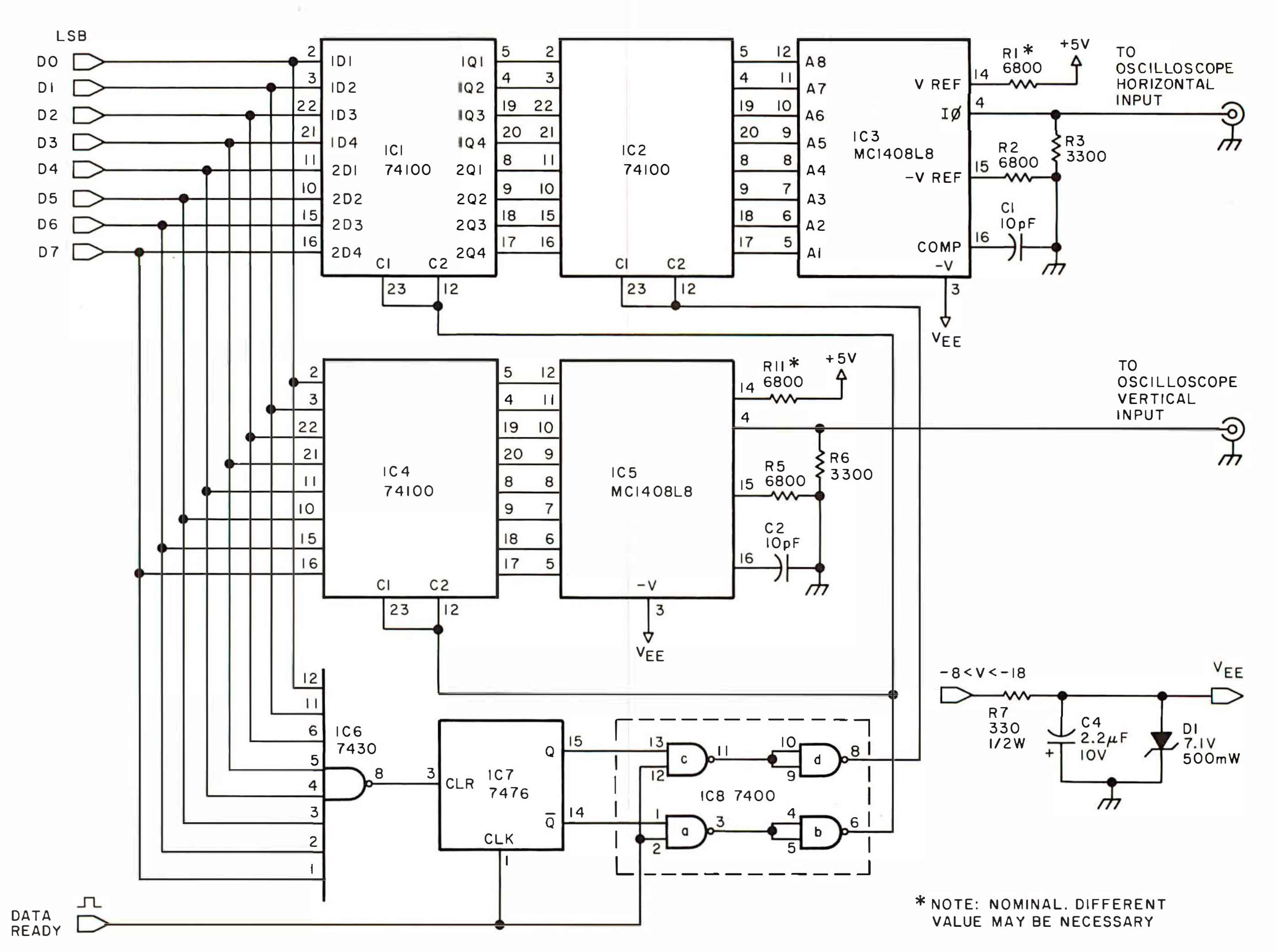


Figure 4: XY oscilloscope display driver. Two digital to analog converters (IC3 and IC5) drive the oscilloscope horizontal and vertical inputs by converting digital data from the computer's output port into voltages. Horizontal and vertical data bytes are routed to their respective converters based on the status of flip flop IC7, which is controlled by the data ready line.

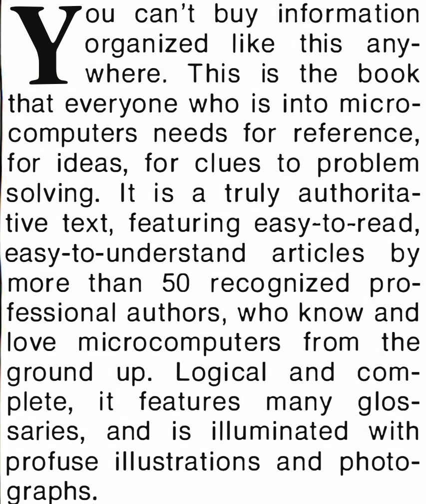
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Circle 316 on inquiry card.

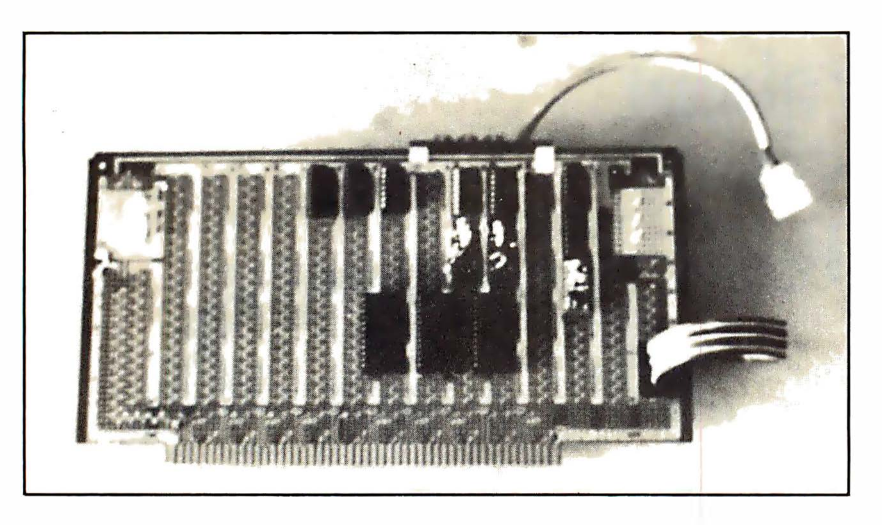


Photo 6: Prototype board for the 3-D interface constructed on an Altair (S-100) bus prototyping card.

the "Beer Budget" graphic display, to which we are indebted.

The data ready pulse is now used to toggle a flip flop (IC7). A byte output when the flip flop is high will go to a storage latch for the X byte (IC1), while the succeeding output byte will be strobed into the Y storage latch (IC4). At the same time as the Y value is stored, the previous X byte is transferred to another latch (IC2) for display. IC2 and IC4 are both connected to 8 bit digital to analog converters (ICs 3 and 5) which will change their output values simultaneously. It may be necessary to substitute slightly different values for the $+V_{REF}$ resistors (R1 and R4) to obtain a linear output from the digital to analog converters.

A special condition of all 1s on the data input lines is detected by a NAND gate (IC6) and used to reset the XY flip flop to the Y state. This insures that the next byte from the output port will be the X byte of an XY pair.

This interface circuit, along with the opto-coupler interface, was wire wrapped on an Altair (S-100) bus prototyping card seen in photo 6. Only supply voltages were brought onto the card through the Altair (S-100) bus connector. Input and output connections were made through a ribbon cable connected to a dual inline package (DIP) socket.

[X_1]
[Y_1]
[X_2]
[Y_2]
[0]
[FF]
[X_3]
[Y_3]
.
.
.

Table 1: Structure of the display table used to store the locations of points to be displayed on the oscilloscope screen. The points are represented by successive X and Y values; empty locations are represented by hexadecimal (00, FF).

Software Control

The locations of points to be displayed on the oscilloscope screen are stored in a display table as shown in table 1. This table consists of a series of XY pairs in successive locations in memory. Unused locations in the table are indicated by an XY coordinate pair, hexadecimal (00,FF). The FF value automatically sets the XY flip flop to the Y state. These unused locations in the table are all displayed at the same point in a corner of the screen. To prevent this point from being displayed, the X and Y positions of the oscilloscope should be adjusted until the point is just out of the display field. Alternatively, the output from IC6 (see figure 4) could be used to gate a Z axis (intensity modulation) signal on the screen, but this is not convenient on many oscilloscopes.

Several small machine language routines were written to provide support for BASIC software (see listing 1). Level 1 Digital Group MaxiBASIC provides several unused pages in low memory for machine language routines. The pages shown in these listings are particular to this level of MaxiBASIC. Linkage to these routines is through the extended BASIC function:

Y = CALL(A [,X])

A is the 16 bit address of the machine routine. X is an optional 16 bit argument passed to the called routine in the DE register pair. The value of the function is contained in the HL pair when the routine returns; in many cases the routine will not return a computed value and the returned value stored in Y will be ignored by the programmer. Other registers need not be preserved.

The first routine, SYNC, is a synchronization routine that waits for a rising edge on the input line from the opto-coupler. The routine first waits for a zero level, then waits for a one level. While waiting, the routine increments register pair HL, which provides a count of the number of cycles spent in the wait loop. Since the routine returns only after the transition from a zero to a one, two successive calls to SYNC will return in HL the number of wait loops in one complete revolution of the mirror (the value in HL from the first call is ignored since the position of the mirror when the routine is called is unknown). The increment DE instruction is added to the wait loops as a do nothing instruction which will lengthen the loop timing to 40 machine cycles. This is exactly the number of cycles required to output an XY pair with the OTIR instruction. The returned value in HL thus gives the waiting time in terms of the number of points which can be displayed in the same amount of time.

A timing routine, TIME, consists of two successive calls to SYNC.

The routine TSTORE sets up the parameters for clearing and displaying the display buffer. In this case, this consists of storing the number of 256 byte pages in the display buffer, passed in DE, into storage location NPAGE.

The next routine, DISP, displays the display buffer. The buffer address is passed in DE. NPAGE, assumed to be set by a call to TSTORE, controls the number of OTIR calls.

Register B will be zero at the beginning of each OTIR instruction, indicating 256 bytes to be transferred. Register E is loaded from NPAGE to hold the total number of pages. Register C contains the output port number.

Routine FILL uses the block transfer instruction LDIR to rapidly clear the display buffer. It is assumed that the number of pages has been preset by a call to TSTORE, and that the first two locations of the buffer contain the desired byte pair to fill the table. The address of the table is passed in DE when FILL is called. This address is moved to HL. Register DE is then incremented twice. The LDIR instruction moves the contents of the location addressed by HL to the location addressed by DE, increments HL and DE, decrements BC, and continues if BC is nonzero. Thus the first and second locations in the table will be transferred to the third and fourth, which will in turn be transferred to the fifth and sixth, etc. Since for a string of n words only n-2 moves are necessary, BC is set to two less than the number of elements in the table.

Initialization Routines

Listing 2 gives a simple BASIC program to put up a display. The first few lines of the program are initialization statements, which routines set up the display table and compute various parameters for the display construction. Normally, they will begin any BASIC routine to drive the spinning mirror. Many of the statements are specific to the current revision of Digital Group MaxiBASIC, since they make use of knowledge of the memory allocation used by the BASIC interpreter.

Since it was desirable to be able to run the program on a minimum Digital Group MaxiBASIC system (18 K bytes), with MaxiBASIC extending up to 13 K, we used BASIC arrays for the display buffer. Extra memory would have permitted dedicated areas in high memory addresses to be used with the knowledge that BASIC would never extend up to these areas. This would have permitted cleaner code, but the more complicated code required is a useful lesson in the incorporation of the internal data structures of an operating system into the code of a higher level language.

A string in MaxiBASIC consists of a series of 1 byte elements. The maximum number of elements is given by the DIM statement for the string, but the actual length of the string may vary dynamically as the program executes, becoming any length from zero elements (an "empty" string) to the maximum stated in the DIM statement. When the DIM statement is executed, an empty string

Listing 1: Assembly language and machine language versions of five utility programs called by the programs in listings 2 and 3. The latter two programs create 3-D images in the rotating mirror (photo 4). SYNC is a synchronization routine that examines the input from the opto-coupler and counts the number of wait loops in one complete revolution of the mirror. Routine TIME consists of two successive calls to SYNC. This is necessary because SYNC may count a partial revolution on the first call. TSTORE sets up the parameters for clearing and displaying the display buffer. DISP displays the display buffer, and FILL uses the Z-80 block transfer function LDIR to rapidly clear the display buffer.

```
                    ;
                    ;  SYNCHRONIZATION ROUTINE
                    ;
                    ;     WAIT FOR RISING EDGE FROM
                    ;     OPTO ISOLATOR CONNECTED TO BIT ZERO
                    ;     OF PORT 2
                    ;
                              ORG   0B00H
B00 21  00  00      SYNC:     LD    HL,0
B03 23              SL1:      INC   HL           ;INCREMENT TOTAL NUMBER OF CYCLES
B04 13                        INC   DE           ;WASTE SOME TIME
B05 DB  02                    IN    A,2          ;INPUT SYNCHRONIZATION BYTE
B07 CB  47                    BIT   0,A          ;AND CHECK BIT 0
B09 C2  03  0B                JP    NZ,SL1       ;NOT ZERO, LOOP BACK
B0C 23              SL2:      INC   HL           ;DUPLICATE ABOVE CODE
B0D 13                        INC   DE
B0E DB  02                    IN    A,2
B10 CB  47                    BIT   0,A
B12 CA  0C  0B                JP    Z,SL2        ;BUT WAIT UNTIL BIT IS ONE
B15 C9                        RET
                    ;
                    ;
                    ;  TIMING ROUTINE
                    ;
                    ;     GET TIME BETWEEN TWO SYNC MARKS
                    ;
                              ORG   0B20H
B20 CD  00  0B      TIME:     CALL SYNC
B23 CD  00  0B                CALL SYNC
B26 C9                        RET
                    ;
                    ;
                    ;  STORAGE ROUTINE
                    ;
                    ;     STORE NUMBER OF PAGES IN DISPLAY BUFFER
                    ;
                              ORG   0B28H
B28 7B              TSTORE:   LD A,E
B29 32  2D  0B                LD (NPAGE),A
B2C C9                        RET
B2D 00              NPAGE:    DB    0
                    ;
                    ;  DISPLAY ROUTINE
                    ;
                    ;     DISPLAY BUFFER USING BLOCK OUTPUT INSTRUCTION
                    ;
                              ORG   0B30H
B30 D5              DISP:     PUSH  DE           ;PUSH PAGE ADDRESS
B31 CD  00  0B                CALL SYNC          ;WAIT FOR SYNC EDGE
B34 E1                        POP   HL           ;POP ADDRESS
B35 0E  02                    LD    C,2          ;LOAD PORT ADDRESS
B37 06  00                    LD    B,0          ;LOAD COUNT (256)
B39 3A  2D  0B                LD    A,(NPAGE)    ;LOAD PAGE COUNT
B3C 5F                        LD    E,A
B3D ED  B3          DL1:      OTIR               ;OUTPUT ONE PAGE
B3F 1D                        DEC   E            ;DECREMENT NUMBER
B40 20  FB                    JR    NZ,DLI       ;RECYCLE IF NOT DONE
B42 C9                        RET

                    ;
                    ;  FILL ROUTINE
                    ;
                    ;     FILL ENTIRE DISPLAY BUFFER WITH CONTENTS OF FIRST TWO BYTES
                    ;     NPAGE MUST BE SET BY A PREVIOUS CALL TO TSTORE
                    ;
                              ORG   0B48H
B48 62              FILL:     LD    H,D          ;MOVE PAGE ADDRESS
B49 6B                        LD    L,E
B4A 13                        INC   DE           ;DESTINATION ADDRESS
B4B 13                        INC   DE           ;IS TWO HIGHER
B4C 3A  2D  0B                LD    A,(NPAGE)    ;NUMBER OF PAGES TO MOVE
B4F 47                        LD    B,A
B50 05                        DEC   B            ;SUBTRACT TWO
B51 0E  FE                    LD    C,0FEH       ;FROM TOTAL NUMBER OF BYTES
B53 ED  B0                    LDIR               ;FILL
B55 C9                        RET
                    ;


0B00 / 21  00  00  23  13  DB  02  CB
0B08 / 47  C2  03  0B  23  13  DB  02
0B10 / CB  47  CA  0C  0B  C9  00  00
0B18 / 00  00  00  00  00  00  00  00
0B20 / CD  00  0B  CD  00  0B  C9  00
0B28 / 7B  32  2D  0B  C9  00  00  00
0B30 / D5  CD  00  0B  E1  0E  02  06
0B38 / 00  3A  2D  0B  5F  ED  B3  1D
0B40 / 20  FB  C9  00  00  00  00  00
0B48 / 62  6B  13  13  3A  2D  0B  47
0B50 / 05  0E  FE  ED  B0  C9  00  00
READY
```

Listing 2: A BASIC program (written in MaxiBASIC) to create a 3-D "square spiral" (see photo 1).

```
READY
LIST 10,330

10 A=26624-FREE(0)
20 DIM S$(5000)
30 N9=EXAM(A-3)
40 N1=N9*128
50 S$=CHR$(0)+CHR$(255)
60 FILL A-1,N9
70 D=CALL(11*256+40,N9)
80 D=CALL(11*256+72,A)
90 REM
100 REM COMPUTE AND DISPLAY BORDER OF DISPLAY
110 DATA 1,0,0,1,-1,0,0,-1
120 S=8
130 X=0
140 Y=0
150 K=1
160 FOR N=1 TO 10
170 RESTORE
180 FOR E=1 TO 4
190 READ X1,Y1
200 FOR S1=1 TO 31
210 X=X+S*X1
220 Y=Y+S*Y1
230 S$(K,K)=CHR$(X)
240 S$(K+1,K+1)=CHR$(Y)
250 K=K+2
260 NEXT S1
270 NEXT E
280 NEXT N
290 REM DISPLAY BUFFER BY REPEATED CALLS TO DISP
300 #"DONE"
310 D=CALL(11*256+48,A)
320 GOTO 310
330 END
READY
```

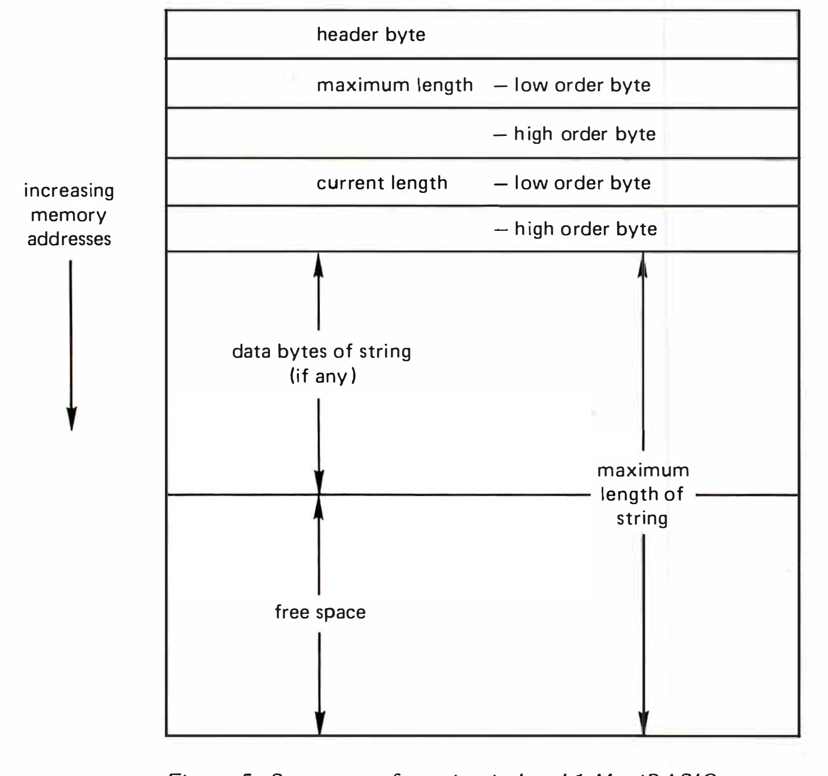


Figure 5: Structure of a string in level 1 MaxiBASIC.

is created at the first available location in memory. The string is stored in memory as a header byte, followed by two bytes giving the maximum length of the string, two bytes giving the current length of the string, and finally the data bytes of the string itself. This structure is shown in figure 5.

The MaxiBASIC function FREE(0) returns the current amount of available memory. This available memory is expanding and contracting during the execution of the program as memory for new variables are allocated and scratch areas for intermediate results are allocated and released. By experimentation, it was found that the statements

10 A=26624–FREE(0)
20 DIM S $(5000)

at the beginning of a program left A pointing to the first data byte of the string S$, here shown arbitrarily as 5000 elements long. The number 26624 (26X1024) is the total number of memory bytes in our system.

The maximum available number of pages is determined in line 30 of listing 2 by examining the beginning of the string S$. This is used to compute the maximum number of XY pairs in the buffer by noting that 128 pairs are in each page. Variable N1 holds the result of this computation. The first two locations in the string S$ are set to the default values of a blank point by statement 50. The length of S$ is adjusted by the FILL statement in line 60. Location NPAGE in the assembly routine area is set to the number of pages by statement 70. Routine FILL is called in statement 80 to clear the data bytes of S$ to an empty display buffer.

One of the easiest displays to set up is an illumination of the borders of the display. The remainder of the program in listing 2 fills successive locations in the display table with the addresses of points around the border of the oscilloscope screen. After the table is filled, the program displays the buffer with repeated calls to DISP.

A photograph of a typical display using this routine is shown in photo 5. This display shows, at the same time, the available display volume for a given configuration of the mirror and screen, the number of points available in the display buffer, and the effects of various motor speeds and synchronization angles. It is a good way to experiment with the physical configuration of the display before going on to more sophisticated displays.

The illuminated edge display is converted

by the spinning mirror into a true three-dimensional display. Since the outside edge of the screen is illuminated, the very edges of the available display volume will be displayed. Manipulation of the relative positions of the oscilloscope screen and the mirror will show the possible display volumes in different orientations before you settle on a final position. Different positions and angles for the screen give display volumes of different sizes and shapes.

Since the display buffer is full, the highest possible point density is displayed. This makes it possible to judge the best tradeoff of flicker rate versus high point density at various motor speeds.

Computation of Point Locations

Figure 6 shows the orientation of the 45° mirror with respect to the oscilloscope screen. The mirror rotates about the Z axis and the screen is perpendicular to the X axis. Suppose we wish to display a point at a certain location. It is then necessary to compute the location of a point on the display

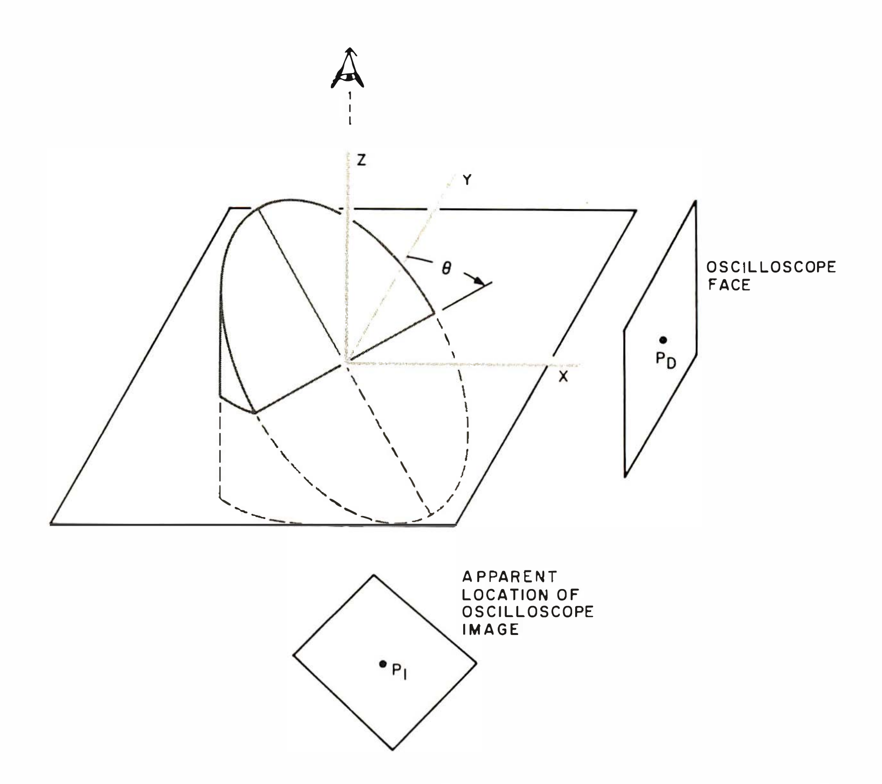


Figure 6: Orientation of the diagonally sliced spinning mirror. The mirror is rotated by an angle θ about the Z axis; the screen is perpendicular to the X axis. To compute a point at a certain location, it is necessary to compute the location of a point on the display screen and a mirror angle which will create a reflection at the desired location.

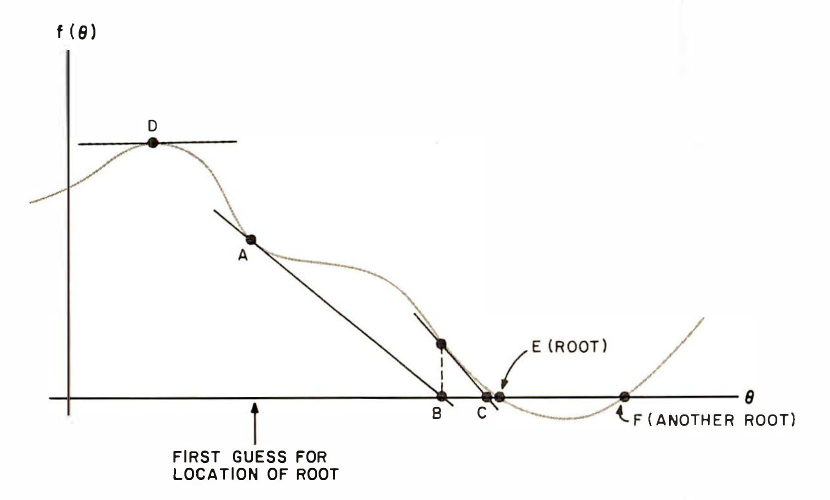


Figure 7: The Newton-Raphson method for determining the roots of an equation. One of the steps necessary in order to calculate the mirror angle for a given point in the 3-D display is to find a particular root of the equation $f(\theta) = -X_i \sin^2\theta + Y_i \sin\theta\cos\theta + Z_i \cos\theta + X_d = 0$. *One way to calculate the desired root is to use the Newton-Raphson method: a first guess is made of the location of the root (ie: where the function crosses the X axis); the guess (point A) is obviously wrong, so the first derivative of the function is calculated and then evaluated at the point guessed. This gives the slope of the function at that point (point A). The process is repeated, but this time following the slope line down to the X axis to determine the next guess (point B). After a few iterations, the value converges rapidly to the root at point E. Complications can occur if a second root of the function is possible, as at point F in this example, or if the slope is too flat, as at point D.*

screen and a mirror angle which will create a reflection at the desired location. Depending on the location and size of the screen, of course, there may not be a point that will create the desired image point. For a given image point (X_i, Y_i, Z_i), the equations for the corresponding display point (X_d, Y_d, Z_d) are:

$$X_d = X_i \sin^2\theta - Y_i \sin\theta \cos\theta - Z_i \cos\theta \qquad (Eq\ 1)$$

$$Y_d = -X_i \sin\theta \cos\theta + Y_i \cos^2\theta - Z_i \sin\theta \qquad (Eq\ 2)$$

$$Z_d = -X_i \cos\theta - Y_i \sin\theta \qquad (Eq\ 3)$$

$$X_i = X_d \sin^2\theta - Y_d \sin\theta \cos\theta - Z_d \cos\theta \qquad (Eq\ 4)$$

$$Y_i = -X_d \sin\theta \cos\theta + Y_d \cos^2\theta - Z_d \sin\theta \qquad (Eq\ 5)$$

$$Z_i = -X_d \cos\theta - Y_d \sin\theta \qquad (Eq\ 6)$$

We know that the display point must lie on the face of the screen, which is at a fixed location on the X axis. This gives us an equation we can solve to find a mirror angle for the display:

$$f(\theta) = -X_i \sin^2\theta + Y_i \sin\theta \cos\theta + Z_i \cos\theta + X_d = 0 \qquad (Eq\ 7)$$

One method we can use to solve this equation is known as Newton's method (also known as the Newton-Raphson method). It is frequently used to compute other mathematical functions such as square roots. Suppose we have an equation, like equation 7 above, which gives a value for any input value of some number θ. We want to find a value of θ for which the computed function is zero (called a *root* of the equation). Figure 7 shows a plot of a function we might be testing. Suppose we start our search for the solution by checking point A. The value of the function here is too high, but we can use it to make an educated guess about the next point to try. This is done by computing the slope of the function at point A and extending the slope down to the horizontal axis (point B). This intersection point becomes the location for the next guess. If the function is a straight line, this one computation will give the right answer. If the curve is not changing very much from a straight line, it will still be a very close estimate. From this new starting point, another guess may be computed (point C). The process is repeated until the answer is close enough to zero to be satisfactory.

One potential problem with this method is that an estimated point may be chosen for which the slope is too flat (point D, for example). This gives a new value that is much too far away; in this case it is better to move over slightly on the curve and try the computation again. Another limitation of the method is that only one zero value will be found at a time, although there may be more than one root of the equation (point F in figure 7, for instance). In our case, a mirror angle may be found which requires that the display point be off the face of the oscilloscope screen even though there is another angle that gives a usable display point.

The slope of equation 7 at a given θ is computed by finding its first derivative:

$$f'(\theta) = -2X_i \sin\theta \cos\theta + Y_i (2\cos^2\theta - 1) - Z_i \sin\theta \qquad (Eq\ 8)$$

and evaluating it for the given θ.

Once the slope is computed, a new value for an estimate of the mirror angle is computed using the equation:

$$\theta_{n+1} = \theta_n - \frac{f(\theta_n)}{f'(\theta_n)} \qquad (Eq\ 9)$$

Listing 3 gives a complete BASIC program to put up a three-dimensional line drawing. The sample DATA statements at the end of the program draw a small house with a tree, shown in a stereo view in photo 3.

The initialization statements discussed above are in lines 10 thru 90. A call to TIME in line 140 returns the total number of display points in one revolution into variable N2. The location and size of the screen is then read into the variables X0, Y0, Y1, Z0, and Z1.

The location of the point displayed when both the X and Y digital to analog converters are set to zero is (X0, Y0, Z0), using the orientation shown in figure 6. Note that in this orientation, the X digital to analog converter moves points in the Y axis and the Y digital to analog converter moves points in the Z axis. The size of the screen is given by variables Y1 and Z1, with the *sign* of these variables indicating the direction in which points move when the values to each digital to analog converter increase. For the interface used in this demonstration, a 4 by 4 inch (10 by 10 cm) display is generated with the zero point in the upper right corner; Y1 and Z1 are thus 4 and −4, respectively.

The next variable read, N3, is the angle in degrees of the mirror when the timing mark is sensed. This angle is converted to radians in line 170. Line 190 then reads the location of the origin of the plot into variables X(1), X(2), and X(3). This is the location of the point in three-dimensional space which will be referred to as (0, 0, 0) during the plot. All locations given in the plotting commands which follow are given relative to this origin. Being able to specify the location of the beginning of the plot makes it easy to move the display to different locations in space.

Choosing an origin for the plot can be tricky, since the screen reflects into a curved volume as the mirror rotates. Running the border display program above can help give an estimate of a good starting point. Another method is to use equations 4, 5, and 6 to compute the reflected position of the center of the oscilloscope screen at several different mirror angles, and to use these as starting points for the display.

The remaining data statements are a series of plot commands. These consist of an integer command code, which may be followed by additional numbers.

The resolution code (−1) is followed by a floating point number giving the spacing between points when drawing lines. This is stored in variable D2.

A plotting command code (1 or 2) is followed by the coordinates, in inches, of the location of the end of the next line. If the code is a 1, dots will be computed and displayed along a line from the coordinates of the last command (stored in X6, Y6, and Z6) to the coordinates in the present command (stored in X5, Y5, and Z5). The dots will be spaced accordingly to the resolution parameter D2. If the code is a 2, the current location will be moved to the indicated point, but no points will be drawn. This is used to move to the start of a new line when no connection is desired with the last line. These commands are similar to motions with the pen down or up on a conventional plotter.

The end code (9999) indicates that all the lines are drawn and that the completed image may be displayed.

Listing 3: A BASIC program (written in MaxiBASIC) to create a 3-D house (see photo 3).

```
READY
LIST

10 A=26624-FREE(Ø)
20 DIM S$(5ØØØ)
30 N9=EXAM(A-3)
40 N1=N9*128
50 S$=CHR$(Ø)+CHR$(255)
60 FILL A-1,N9
70 D=CALL(11*256+40,N9)
80 D=CALL(11*256+72,A)
90 REM
100 REM DRAW PROGRAM 8/1/77
110 REM
120 REM DRAW A SERIES OF POINTS IN STRAIGHT LINES ON THE SPINNING
130 REM  MIRROR USING PLOTTER-LIKE COMMANDS
140 N2=CALL(11*256+32)
150 REM
160 READ XØ,YØ,Y1,ZØ,Z1,N3
170 N3=-N3/18Ø*3.14159
180 REM READ ORIGIN
190 READ X(1),X(2),X(3)
200 REM READ COMMAND
210 READ NØ
220 IF NØ=9999 THEN 460
230 IF NØ=-1 THEN 440
240 REM PLOTTING TO NEW POINT, READ IN COORDINATES
250 READ X5,Y5,Z5
260 IF NØ=2 THEN 420
270 IF NØ<>1 THEN 500
280 REM DRAW FROM OLD TO NEW WITH SPACING OF D2
290 REM COMPUTE NUMBER OF POINTS IN N5 AND SPACINGS IN X7, Y7, Z7
300 D=SQRT( (X6-X5)↑2 + (Y6-Y5)↑2 + (Z6-Z5)↑2 )
310 N5=INT(D/D2)+1
320 X7=(X5-X6)/N5:Y7=(Y5-Y6)/N5:Z7=(Z5-Z6)/N5
330 REM NOW PLOT EACH POINT
340 FOR J=1 TO N5
350 X6=X6+X7:Y6=Y6+Y7:Z6=Z6+Z7
360 X9=X6+X(1):Y9=Y6+X(2):Z9=Z6+X(3)
370 GOSUB 680
380 REM STORE POINT IF CONVERGED
390 IF Z>Ø THEN GOSUB 520
400 NEXT J
410 REM CHANGE LOCATION OF CURRENT POINT
420 X6=X5:Y6=Y5:Z6=Z5
430 GOTO 210
440 READ D2
450 GOTO 210
460 REM PUT UP DISPLAY
470 PRINT "DONE"
480 D=CALL(11*256+48,A)
490 GOTO 480
500 PRINT "BAD PLOT COMMAND"
510 STOP
520 REM LIST STORE ROUTINE
530 REM X AND Y ARE POINTS ON SCREEN; Z IS POSITION IN LIST
540 REM CHECK X AND Y WITHIN BOUNDS
550 IF X>254 OR X<Ø THEN #"X OFF SCALE:";X:RETURN
560 IF Y>254 OR Y<Ø THEN #"Y OFF SCALE:";Y:RETURN
```

Listing 3, continued:

```
570 REM CHECK BYTE NUMBER Z2 ( = Z+Z) IN LIST.
580 REM IF POSITION NOT EMPTY, CHECK NEXT POSITION
590 Z2=2*INT(Z)
600 IF Z2>N1+N1 THEN #"LIST POSN TOO BIG:";Z:RETURN
610 IF ASC(S$(Z2))=255 THEN 640
620 Z2=Z2+2:GOTO 600
630 REM OK POSITION FOUND. STORE
640 S$(Z2-1)=CHR$(X)
650 S$(Z2)=CHR$(Y)
660 #Z2
670 RETURN
680 REM CONVERSION ROUTINE FOR POINTS X9, Y9, Z9
690 REM X0,Y0,Y1,Z0,Z1 ARE ASSUMED TO BE INITIALIZED
700 REM X,Y,Z ARE OUTPUT AS X AND Y ON SCREEN, & LIST POSN
710 REM INITIALIZE LIMITS AND STARTING VALUES
720 N9=20
730 T9=.01
740 F9=.3
750 J9=1
760 REM STARTING ANGLE (T8) WILL BE LAST VALUE COMPUTED TO
770 REM SPEED ITERATION
780 C8=COS(T8) : S8=SIN(T8)
790 REM COMPUTE FUNCTION WHICH IS TO GO TO ZERO
800 F=Z9*C8 + Y9*S8*C8 - X9*S8*S8 + X0
810 REM TEST BELOW THRESHOLD
820 IF ABS(F)<T9 THEN 990
830 REM COMPUTE DERIVATIVE
840 D9=-Z9*S8 + Y9*(2*C8*C8-1) - X9*2*C8*S8
850 REM COMPUTE NEXT STEP WITH NEWTON'S METHOD
860 REM CHANGE BY STANDARD AMOUNT IF DERIVATIVE IS TOO SMALL
870 IF ABS(D9)<.005 THEN D9=.005
880 REM OR STEP WOULD BE TOO BIG
890 F=F/D9:IF ABS(F)>F9 THEN F=F9
900 T8=T8-F
910 REM CHECK TOO MANY ITERATIONS
920 J9=J9+1 : IF J9<=N9 THEN 780
930 #"DIDNT CONVERGE FOR",X9,Y9,Z9
940 REM SET DIDN'T CONVERGE FLAG
950 Z=-1
960 RETURN
970 REM CONVERGED; CONVERT ANGLE TO LIST POSITION MOD N2
980 REM    (N2 = LENGTH OF LIST)
990 Z=(N3-T8)*N2/(3.14*2)
1000 IF Z>0 THEN 1020
1010 Z=Z+N2:GOTO 1000
1020 IF Z<=N2 THEN 1040
1030 Z=Z-N2:GOTO 1000
1040 REM COMPUTE X AND Y POSITION ON SCREEN
1050 REM NOTE THAT X ON SCREEN CORRESPONDS TO Y IN COORDINATE SPACE
1060 REM AND Y TO Z
1070 X=-X9*S8*C8+Y9*C8*C8-Z9*S8
1080 Y=-X9*C8-Y9*S8
1090 REM CONVERT FROM LOCATION IN INCHES TO DAC OUTPUT VALUE
1100 X=250*(X-Y0)/Y1
1110 Y=250*(Y-Z0)/Z1
1120 RETURN
1130 REM ORIGIN AND SIZE OF CRT
1140 DATA 4,-4,4,5,-4
1150 REM ANGLE OF MIRROR AT SYNC
1160 DATA -22
1170 REM RELATIVE ORIGIN OF PLOT
1180 DATA -3,2.5,-5.5
1190 REM RESOLUTION OF PLOT
1200 DATA -1,.15
1210 REM DRAWING OF HOUSE WITH TREE
1220 REM FRAME
1230 DATA 2,1,-1,1
1240 DATA 1,1,-1,0, 1,1,1,0, 1,0,1,0
1250 DATA 1,0,1,1, 1,0,-1,1, 1,1,-1,1
1260 DATA 1,1,1,1, 1,0,1,1, 2,1,1,1
1270 DATA 1,1,1,0, 2,0,1,0, 1,0,-1,0
1280 DATA 1,0,-1,1, 2,0,-1,0, 1,1,-1,0
1290 REM ROOF
1300 DATA 2,0,-1,1, 1,.5,-1,1.5, 1,1,-1,1
1310 DATA 2,.5,-1,1.5, 1,.5,1,1.5, 1,0,1,1
1320 2,.5,1,1.5,1,1,1,1
1330 REM DOOR
1340 DATA 2,.5,1,1.5,1,1,1,1
1350 DATA 2,.4,-1,0,1,.4,-1,.5,1,.6,-1,.5,1,.6,-1,0
1360 REM PATH
1370 DATA 2,.4,-1,0,1,.4,-2,0
1380 DATA 2,.6,-2,0,1,.6,-1,0
1390 REM TREE
1400 DATA 2,1,-1.5,0,1,1,-1.5,1.2
1410 DATA 2,1,-1.5,.2,1,1.4,-1.5,.6
1420 DATA 2,1,-1.5,.4,1,1,-1.15,.65
1430 DATA 2,1,-1.5,.6,1,.7,-1.5,.9
1440 DATA 2,1,-1.5,.8,1,1,-1.75,1.05
1450 DATA 2,1,-1.5,1,1,1.2,-1.5,1.2
1460 DATA 9999
READY
```

These plot commands are decoded in lines 210 thru 270. Lines 280 thru 450 then compute the coordinates of the points to be displayed. The total distance D between the last point and the current one is computed in line 300. This is divided into an integer number of steps, N5, of sizes X7, Y7, and Z7. Then each of the N5 points is generated by calls to two subroutines which store values in a digital to analog conversion table corresponding to each point. Once all points are computed, the coordinates of the current location are stored as the previous one (in X6, Y6 and Z6), and the next command is extracted from the DATA statements.

If the end command (9999) is detected, lines 470 thru 490 are executed. These put up the display by repeated calls to DISP. Another way to generate the display is to use the timing mark to generate an interrupt. In this way the BASIC program may be interrupted during the computation of the display points, and the display buffer may be viewed as it is being constructed. Mixed results were obtained when using this method with MaxiBASIC; some points would be computed incorrectly if a mode 2 hardware interrupt were sensed in the middle of a computation. Another way to view the display buffer as it is being built is to occasionally put up a display for a few revolutions of the mirror.

Coordinate conversion is done in the subroutine in lines 680 to 1120. Variables X9, Y9, and Z9 contain the coordinates of the point to be converted. Variable N9 controls the number of iterations of Newton's method to be attempted until a given accuracy, T9, is reached. The angle of the mirror used in each iteration, T8, is initially set to the last value computed by the conversion routine. Since, frequently, many points will be plotted close together, this is a good first estimate of the angle of the mirror. T8 will be set to zero by MaxiBASIC the first time this routine is entered.

During each iteration, the test function F is computed (line 800). If this is below the tolerance level (T9), the routine has converged and the display points can be computed. Otherwise, the slope D9 is computed (line 840). This is used to compute the next test point in lines 870 to 900.

Once the routine has converged, T8 is converted to the appropriate position, Z, in the display buffer. The values for the X and Y digital to analog converters are then computed from the Y and Z coordinates, respectively, of the image point.

Finally, the computed values are stored

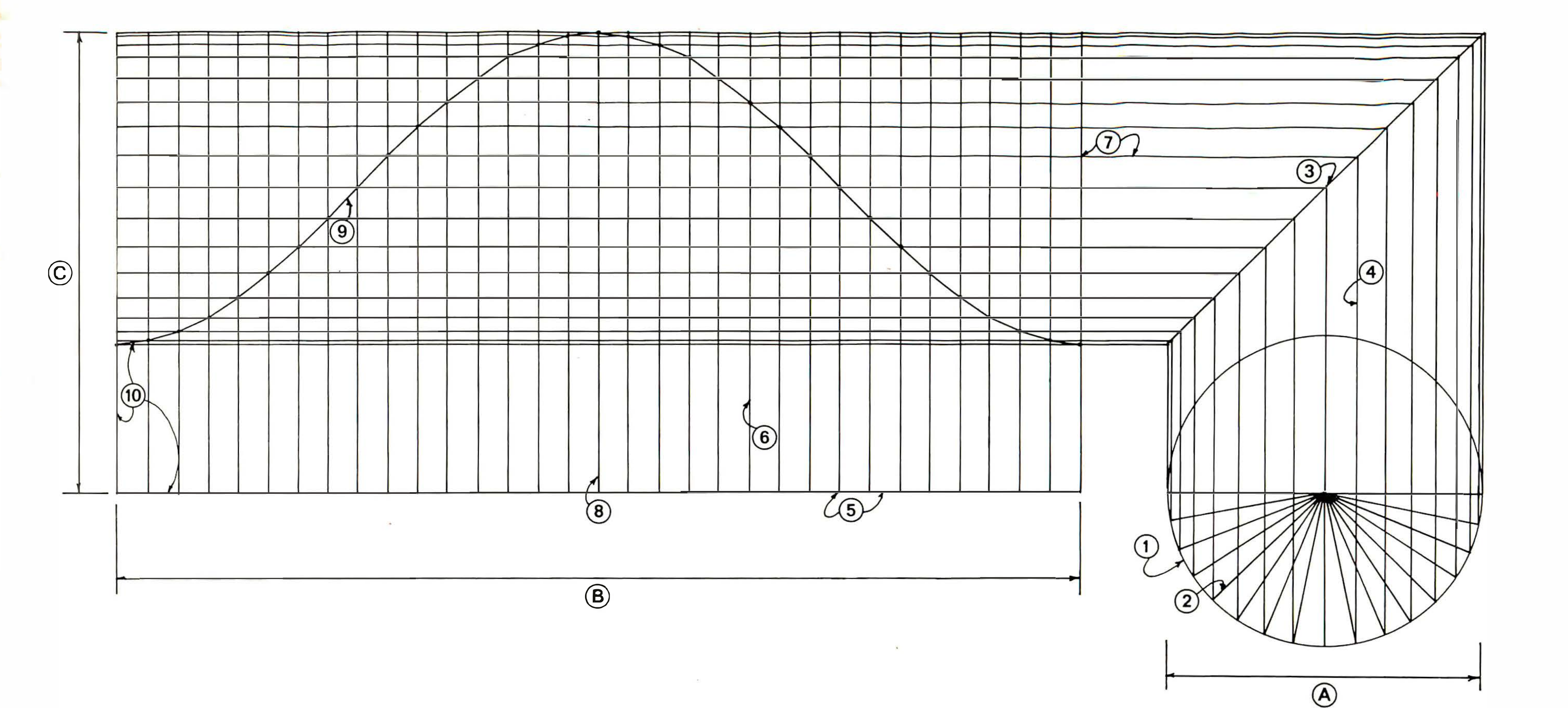


Figure 8: Construction of a template for cutting a 45° angle in a cardboard tube to make a rotating mirror. Details are described in the accompanying text. The circled numbers refer to step numbers 1 thru 10.

Steps for **Cutting a 45° Angle Through a Cardboard Tube**

A = diameter of tube
B = circumference of tube
C = finished height of tube

1. Draw a circle the same size as the outside diameter of the tube.
2. Divide the circle into 32 equal parts of 11¼° each.
3. Draw a 45° angle above the circle.
4. Carry the points at the outside of the circle straight up to the 45° angle.
5. Find the circumference of the circle, draw a straight line, and divide it into 32 equal parts.
6. Carry lines from those divisions straight upward.
7. Bring lines straight across from the intersections at the 45° angle line and intersect with the vertical lines.
8. Starting at the center line, mark points of intersection.
9. Fill in between points of intersection.
10. Cut out pattern and wrap around tube, lining up straight circumference side of pattern with (cut) end of tube square.
11. Carefully trace curved line end of pattern onto tube.
12. Remove pattern from tube and save for making black paper cover for tube.
13. Cut along traced line on tube with an X-acto (or similar) knife.
14. Tape large sheet of sandpaper to a table top or other flat surface.
15. Sand end of tube until flat.
16. Tube is now ready for application of Mylar mirror surface.

in the display buffer in the subroutine from lines 520 to 670. This routine checks that the values for X, Y and Z are within bounds, and stores them in the first empty location in the display buffer after the desired location.

Final Thoughts

We hope this article will encourage readers to experiment with 3-D graphics. The advantages of the technique are immediately apparent when it is demonstrated, and the applications include such areas as computer aided design and architectural planning as well as action games.■

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Constructing the Mirror

The spinning mirror used for the development of the three-dimensional graphics described in this article was machined from a solid block of aluminum. It was produced under the auspices of a National Institute of Health grant, and is obviously an impractical solution to mirror construction for the personal computer experimenter.

We did, however, build an alternate, inexpensive, rotating mirror that is quite adequate for producing three-dimensional images. It uses surplus parts available from the dealers who advertise in this magazine. The rotating mirror element is fabricated by cutting a 45° angle through a short section of cardboard mailing tube of between 3 and 5 inches (7 to 12 cm) in diameter. This angle can be cut using the template shown in figure 8. The piece of mailing tube should be kept quite short. A piece of aluminized Mylar film, available from some art supply houses (or from Edmund Scientific Co, 300 Edscorp Bldg, Barrington NJ 08007), is cut slightly larger than the 45° angle end of the tube. The Mylar is then stretched over the end of the tube and taped to the tube's side. This should be done by first stretching the Mylar along the long axis of the 45° cut and tacking down the Mylar with short pieces of tape, then stretching the Mylar across the short axis and taping that axis down. Then work around the rest of the edge, taping opposite sides, and using care not to produce any wrinkles, until the entire edge is taped down.

Any motor can be used to spin the mirror, as long as it is a type whose speed can be controlled with a Variac or motor speed controller. A flywheel cut from plywood or aluminum and mounted to the motor shaft is attached to the cardboard tube. If a mailing tube can be found with a removable end cap, the cap can be mounted to the flywheel plate and the tube can then simply be slipped into the end cap.

The motor and Variac should be mounted inside a sturdy enclosure. The motor shaft should project up through a hole in the enclosure; the flywheel and tube are then mounted to the shaft outside the enclosure. Motor, flywheel and tube should be carefully centered and balanced. The template for cutting the 45° angle through the tube can also be used as a pattern for a piece of black paper to be glued to the outside of the tube. The motor enclosure should be painted black to minimize reflections.

If the motor used has a shaft at both ends of the motor housing, a black disk, 3 inches (7 cm) or so in diameter, can be attached to the shaft inside the enclosure. The reflective opto-coupler described in the article can be mounted to the inside of the enclosure in close proximity to the edge of the disk. A piece of white tape applied to the edge of the disc will then trigger the opto-coupler each time the motor makes a revolution. If the motor only has a shaft at one end, the opto-coupler will have to be mounted outside the enclosure, with the piece of white tape fastened to the cardboard tube. Guard against ambient light triggering the opto-coupler if the latter method is used.

Light baffles and shields for the mirror should be experimented with; caution should be observed around the spinning mirror, as with any piece of moving machinery.

William Harris

Continued from page 22

set conversion: the ATV Research "Pixe-Verter," which uses the radio frequency (RF) modulator method, and the Pickles and Trout TVM-04, which uses the direct video entry technique.

The RF modulator method has the advantages of simplicity and generality. The modulator circuit is easy to construct, and no modifications to the TV set are required. The circuit board can be mounted inside your computer or other video source, and any TV set can be used simply by clipping two wires onto the antenna terminals. The disadvantages are that the number of characters that can be displayed across a line is limited, and that certain precautions must be taken to avoid trouble with the Federal Communications Commission.

When a video signal is used to modulate a very high frequency RF signal which is then fed through the receiver circuits of a TV set, bandwidth limitations are encountered. The practical limit is about 3.5 MHz, which is enough to display at most about 32 characters per line. Photo 1 shows the kind of display you can expect when using an RF modulator such as the Pixe-Verter. The video source here is an Ohio Scientific Instruments Model 440B video board, and the television set is a Hitachi Model PA-8, purchased new for about $90 from a discount house in Boston MA.

When assembled, the Pixe-Verter legally becomes what the FCC calls a "Class 1 TV device." Since the device is actually a tiny TV broadcast transmitter, the FCC doesn't want you to broadcast signals which will create interference on your neighbor's TV sets. Actually, the device is so low powered that in my experience interference is scarcely noticeable on a TV set more than a few feet away. The unit should be enclosed in a metal box (a typical personal computer cabinet is fine), and shielded cable should be used to connect the unit to the TV set. Photo 2 shows the Pixe-Verter mounted in the space provided on the OSI 440B video board. The unit requires a -5 to -6.5 V supply, but this can be obtained by isolating the printed circuit board from the video board and reversing the power connections from the computer's +5 V supply.

The simplicity of the RF modulator method, as compared with the direct video entry method, can be illustrated by compar-

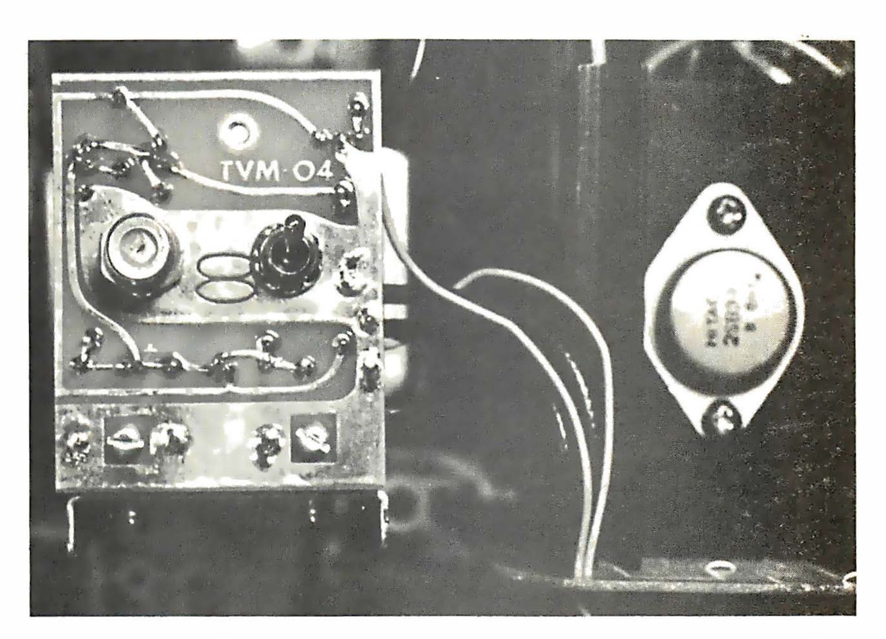


Photo 3: This inside view of the Hitachi Model PA-8 television set shows how the TVM-04 printed circuit board is mounted on the metal frame near the power transformer.

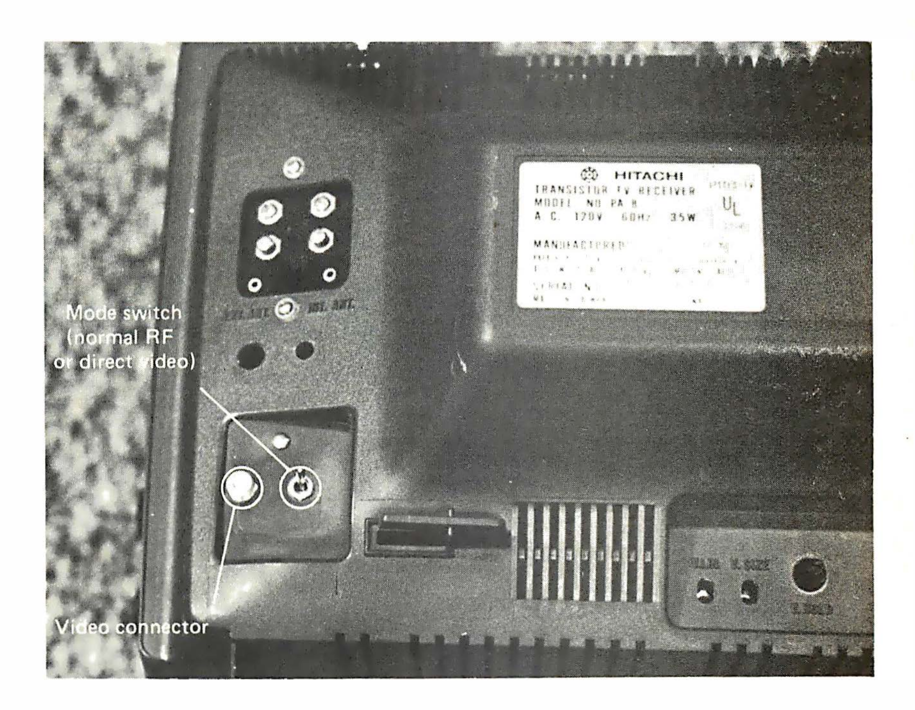


Photo 4: The TVM-04 lines up with the back of the TV set's plastic cabinet, giving access to a shielded cable connector for the video signal and a switch for selecting either normal program viewing or the computer generated display.

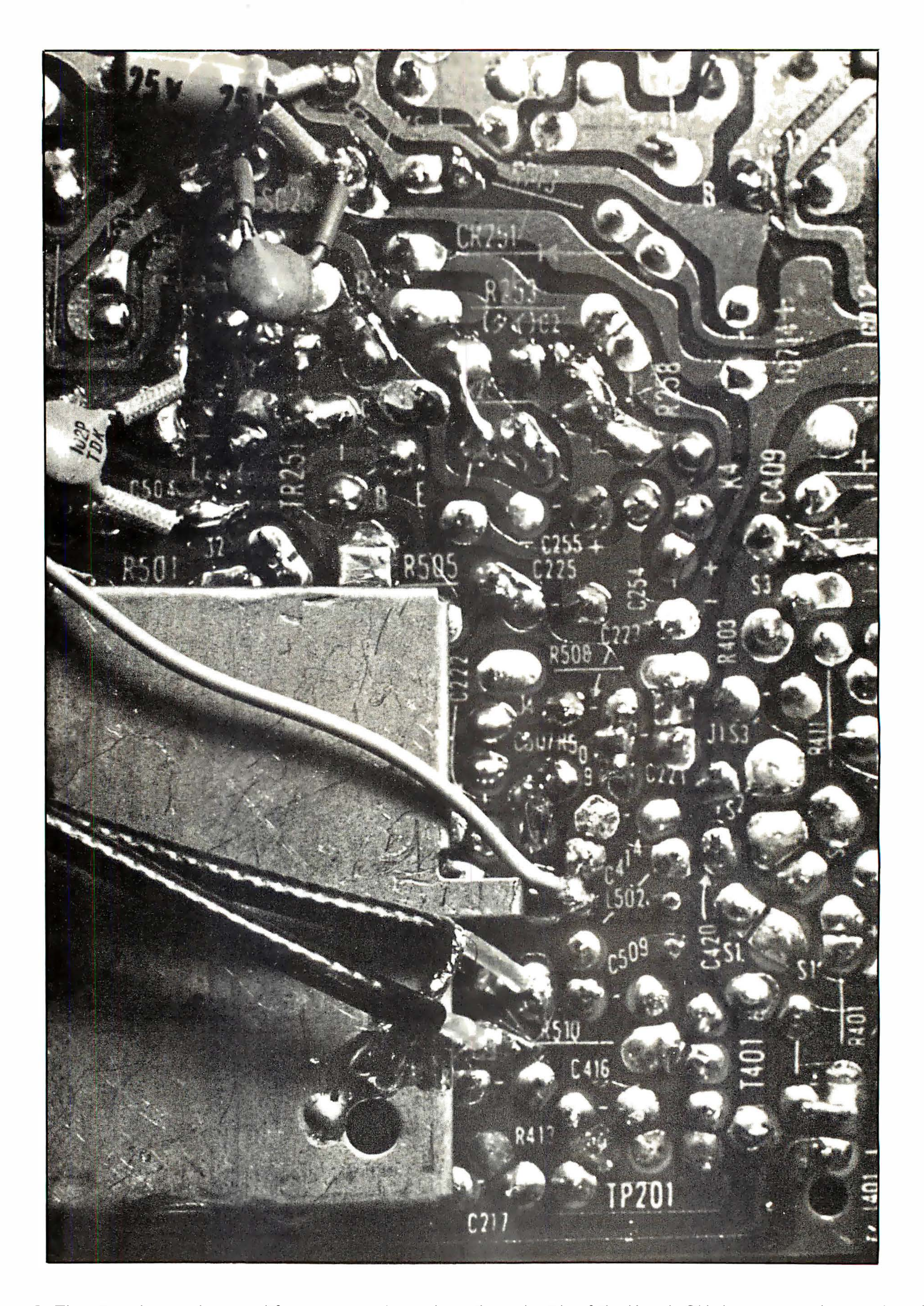


Photo 5: This view shows where modifications must be made to the underside of the Hitachi SX chassis printed circuit board. A foil trace carrying the video signal is cut and routed through shielded wire to the external switch, and a small disk capacitor (at top with spaghetti tubing on legs) is attached across a spark gap to improve the set's response to abrupt black and white changes.

ing the instructions that come with the Pixe-Verter (eight steps listed on one page) with the instructions supplied with the Pickles and Trout TVM-04 (51 very detailed steps on six pages). The direct video entry instructions also require you to drill holes in metal and plastic, cut a printed circuit board foil trace while being careful not to scratch other foil traces a quarter of an inch away, and remove a molded plastic boss with a hot knife or other instrument. Moreover, when working inside the TV set cabinet, there is some danger of accidental breakage and implosion of the TV picture tube! Direct video entry is not for the person who has never soldered before. If you are in this position, ask your friendly local computer store to help you. But the experienced hobbyist can put together the Pickles and Trout kit without hazard in about half a day, and the results are well worth it.

I bought the Hitachi Model PA-8 TV set with the intention of eventually converting it to direct video entry, since the Pickles and Trout TVM-04 is specifically designed for use in sets with the Hitachi SX chassis (Models P-03, P-04, P-05, P-08, P-53, P-63, etc). The design of this set facilitates switching between normal program viewing and direct video entry, and provides sufficient bandwidth to display as many as 96 characters on a line. The TVM-04 is mounted on the TV set's metal frame near the power transformer, as shown in photo 3, and lines up with a flat area on the set's plastic case to provide a professional looking external switch and shielded cable connector (see photo 4). Shielded wires are run to the point on the set's printed circuit board where the foil was cut, and a small capacitor is also soldered across a spark gap to limit the overshoot and ringing of the video amplifier when the video signal abruptly changes from black to white (see photo 5). For comparison, photo 6 shows the same video source as photo 1, using the same Hitachi TV set as photo 1, but with the direct video entry mode. As one would expect, the display is much clearer, more legible and more stable than the display obtained with the Pixe-Verter. For what it's worth, the two methods can be used together: I can view either of two computer generated displays at the flick of a switch!

One consideration that must be borne in mind when using the TVM-04 is that the modifications to the set void the manufacturer's warranty. Hence it pays to postpone making the modifications until you have owned and operated the set for a while and are sure that it is working pro-

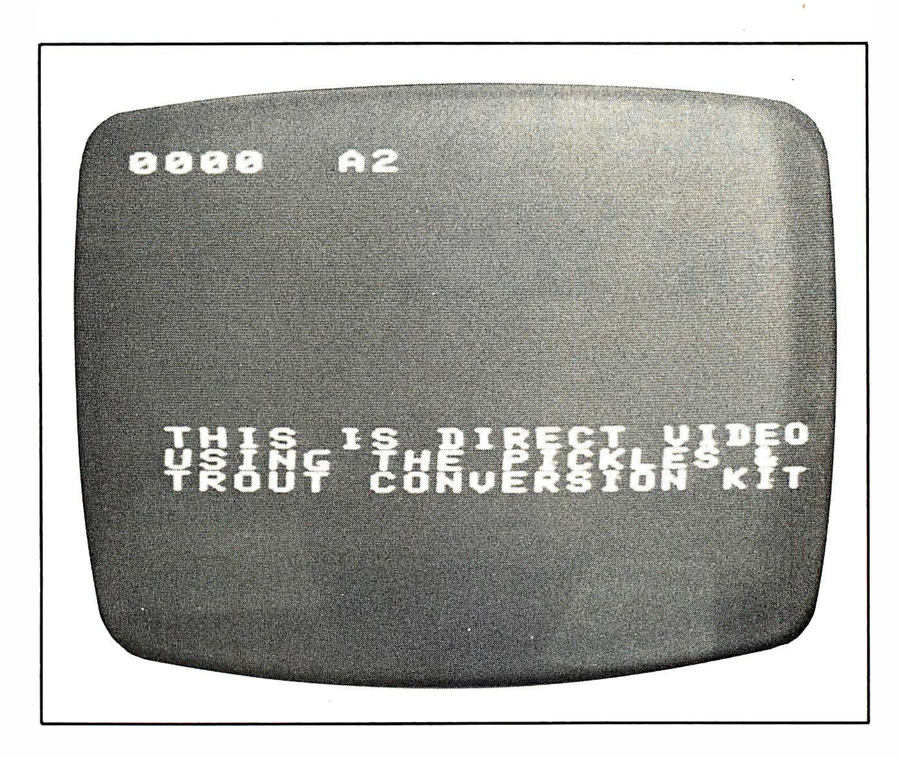


Photo 6: The same display source as that of photo 1, produced on the same TV set, but with the aid of the Pickles and Trout TVM-04. Note the sharpness of this direct video display in contrast to the RF entry of photo 1.



Photo 7: To illustrate the wider field possible with the Pickles and Trout direct video conversion, the 64 character display of a SOL-20 was used with the converted television perched on top of the SOL. We made no attempt to adjust the controls of the television set to remove the overscan condition evident in this photo of the Processor Technology LIFE demonstration program's output.

perly. After this initial "burn-in" period you can be reasonably certain that the set will continue to operate over the life of the warranty, and the modifications can be made. I took this precaution and it paid off. I had trouble with the set during the first week after I bought it, and had it fixed under warranty by a local TV repairman. Some time later I installed the TVM-04 and have had no trouble with it since.

My experience has been that either the RF modulator method or the direct video entry technique can be used with good results. If 32 characters on a line is sufficient, the Pixe-Verter is quite satisfactory. If you want a more dense character display and have some experience with electronics assembly (or someone to help you), do not hesitate to use the TVM-04. I hope this article will help you to make an intelligent choice.■

A note about the photographs: *The photos accompanying this article were made in BYTE's offices with ASA 400 speed 35 mm film in a Vivitar single lens reflex camera with macrolens, tripod, through-the-lens meter, and delayed release shutter. The pictures of the video displays were made with 1/15th second exposure time so that an integer number of 1/30th second television frames would be exposed. The close-up pictures of the internal and external details of the Hitachi television conversion were made with longer exposure times and room light as illumination. In all cases, the delayed shutter release was used so that any mechanical vibrations from manual release would be damped out over the 9 seconds or so delay possible with this feature.*

The Pixe-Verter Model PXV-2A is available for $8.50 postpaid from ATV Research, 13th and Broadway, Dakota City NB 68731. The TVM-04 is $20 from Pickles and Trout, POB 1206, Goleta CA 93018. Similar products for both the RF modulator method and the direct video entry technique are available from Vamp Inc, POB 29315, Los Angeles CA 90029.

Continued from page 8

Atlantic ocean into northern New England. The storm sat in place, and the snow came. And came. And came. Before it was all over, perhaps a full meter of new snow had been deposited over much of southern New Hampshire. Boston and the state of Massachusetts rolled up their sidewalks again and closed down with some 68 cm of snowfall (a previous storm had set local records two weeks earlier, only to be outdone by this new storm).

But the evaluation of such a storm depends upon your point of view. For those fortunate enough to be away from the raging sea and power outages, it is an opportunity. It provides a nice new carpet of snow so that when I go skiing again next weekend the slopes will take on a whole new character. It provides me with the opportunity to spend 20 minutes and cross country ski to the office today.

Yesterday, while the snow was falling and our office was closed, it provided me (and many another personal computer user) with an absolutely superb excuse to stay home with my computers. I spent a quiet day working on the systems software for my new disk drive. During the course of one snowy day I vastly updated my documentation of the systems software, created a new 1 K EROM with low level disk drivers for interrupt driven block transfers between memory and disk, implemented a primitive physical IO operating system to use as a tool in developing the final operating system for my computer, and designed the details of the file system for the new systems software; all in one snowy day which is now called "The Blizzard of '78."

A solitary day in my basement laboratory, isolated by blowing and drifted snow, turned into an unexpected opportunity to steal some time to work on my personal creations. While the rest of the region freaks out over excess snow, a computer experimenter can certainly turn the time to advantage until the storm has blown itself away.

Of course the reality of the snowy day returned at 6:00 this morning when I began to dig out the driveway. But the process of moving the snow is an opportunity: even computer people need a bit of vigorous exercise on occasion.■



Comments on PASCAL, Learning How to Program, and Small Systems

Gary A Ford, Assistant Professor
Dept of Mathematics
Arizona State University
Tempe AZ 85281

The editorial in the December 1977 BYTE asked if PASCAL is the next BASIC. Implicit in this question is the suggestion that personal computing needs a widely used programming language. Ostensibly, this will facilitate exchange of software, and thus help eliminate the existing software vacuum for personal computer systems. Should PASCAL be the language used to begin to fill this void? To answer this question, we should look at the history of PASCAL to see for what purposes it was developed.

Wirth states two principal goals for PASCAL: "to make available a language suitable to teach programming as a systematic discipline based on certain fundamental concepts clearly and naturally reflected by the language," and "to develop implementations of this language which are both reliable and efficient on *presently available computers*" (emphasis added).

With regard to the first of these goals, Wirth contends that "the language in which the student is taught to express his ideas profoundly influences his habits of thought and invention." My experience shows that this is a remarkably accurate statement. I have taught computer science to university undergraduates for several years, and recently taught several intermediate level courses to students with a variety of programming backgrounds. The students had all had two or three quarters of formal computer science courses at the same university during the previous year, and all were familiar with the same computers. However, some had learned to program in BASIC, some in FORTRAN, and some in a structured variant of FORTRAN which included, among other features, two varieties of if-then-else, five varieties of iterative statements, two varieties

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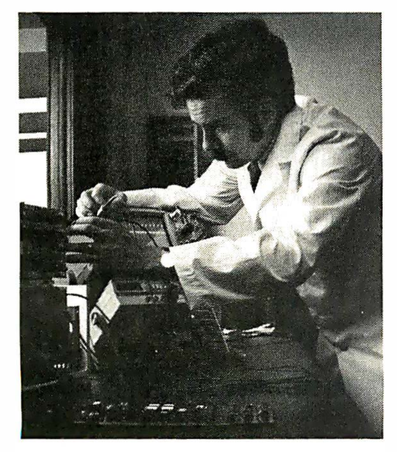
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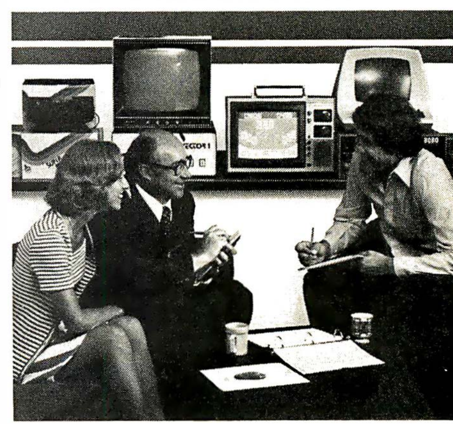
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of multiple branch structures, and a simple but powerful procedure facility. The structured FORTRAN programmers proved to be significantly better performers in the intermediate level courses in all ways. They were much quicker to understand new algorithms, new data structures, and new applications. They were superior in applying this knowledge to new problems, which can, in part, be attributed to the fact that they were not thinking in the narrow terms required in BASIC and FORTRAN. They wrote better programs in assembly language, perhaps again because they could think in structured programming terms. They also, not unexpectedly, learned PASCAL (which was taught in conjunction with a data structures course) much faster than the other students. In fact, some of the BASIC and FORTRAN programmers never did make the transition to PASCAL; they wrote PASCAL programs that looked like line by line translations of BASIC and FORTRAN programs. An informal follow-up of some of these students in more advanced courses showed that the BASIC and FORTRAN group continued to lag behind, especially in courses in analysis of algorithms and design of large systems.

Of course, this was not a controlled experiment, so the conclusions cannot be supported scientifically. However, I believe it is true that since so much of computer science involves abilities to analyze, to organize, and to plan, the thinking process taught in a first programming course, which

in turn depends on the language used, has an enormous impact on the development of computer scientists.

Thus, PASCAL sounds like a good language for beginners (ie: many of today's computer hobbyists). There are other reasons for supporting the spread of PASCAL, including, for example, its outstanding data structuring facilities. Some problems are easily stated and solved in terms of such structures as sets, lists, sequences, trees, or groups of disparate items. PASCAL allows the programmer to define and to deal directly with such structures, whereas BASIC and FORTRAN force the programmer to disguise these structures as arrays. Of course, obscuring the original ideas often leads to obscure program logic.

With regard to Wirth's second goal for PASCAL, we suddenly have a problem. The personal computer systems of today are quite different from the "presently available computers" Wirth had in mind ten years ago. Therefore, some language features that are desirable for present personal computer systems are absent from PASCAL. Perhaps the most important of these features are in the category of access to peripheral devices and processor hardware facilities.

PASCAL has only two primitive IO operations: get and put. Each moves a single unit of data (character, integer, record, etc) from or to a sequential file. Files are not necessarily associated with or stored on secondary storage devices, although two special predefined files (named input and output) are available for those files associated with devices that will also be accessed by humans. There are in addition two predefined procedures (named read and write) that perform data transmission from or to files in particularly useful ways, but it is important to emphasize that these are procedures (subprograms) and not statements or operations in the language.

The peripheral devices of personal computer systems are extremely varied, and very few system configurations are exactly alike. Therefore, each user will need somewhat different IO capabilities in the language. Many users have an on line terminal, access to which requires the ability to access specific absolute addresses in memory or specific port addresses. Users with disks will need direct access file capabilities. Others may want the ability to process interrupts for real time applications. None of these capabilities exist in PASCAL, and none can easily be implemented as a disguised sequential file.

The obvious conclusion is that if a push for PASCAL as *the* language of personal computing is made, there will be a variety of nonstandard implementations. This is exactly what we have seen with BASIC. Each individual implementor will add her own versions of her own favorite bells and whistles. We may expect numerous methods of specifying absolute memory addresses (peeks and pokes), direct access disk file statements, and all kinds of facilities to handle the exotic peripherals being attached to personal systems. In addition, implementors will want to add their own favorite data type (for example, PASCAL does not have a built-in string data type), and their own favorite operator (for example, PASCAL does not have an exponentiation operator). Next, seeing the size of the resulting compiler, implementors will begin to delete their least favorite standard features (often meaning the ones they least understand), in order to come up with a 4 K version of "eensyweensyPASCAL."

One approach to preventing some of the problems just mentioned is to get all of us hobbyists together to agree (is this possible?) on a standard set of additions and deletions, or perhaps a few standard sets in order to develop 8 K, 12 K, 16 K, etc, versions. The traumatization of the language could be minimized by requiring that all the new features be implemented as procedures, rather than as new statement types, thus maintaining the syntactic integrity of the language. Of course, this would require a capability to link external procedures to each PASCAL program, and none of these procedures could be written in PASCAL. This means either that all users will need to know another programming language, or that the implementors of the new varieties of PASCAL will have to supply customized procedures for each customer.

There is a fundamental flaw in this approach, however. PASCAL was not intended to be all things to all people. It was designed with specific, well thought out, predefined goals. All aspects of the language were designed to complement each other in attaining those goals. Any deletion from the language, however minor it seems, will upset this balance, and thus damage PASCAL's ability to achieve its goals. Deletions and additions will also change the character of the language, and it is this overall character of PASCAL that has brought it so many devotees.

A better approach, I believe, is for those of us in personal computing to get together to agree on *principles* for the next widely used language, rather than on the features to add to or delete from an existing language. This is not any kind of vote against PASCAL; to the contrary, I hope PASCAL will become available to all hobbyists with systems that can support *standard* PASCAL, and that it be used for all *suitable* applications programming. I have used PASCAL for at least 95% of my own programming over the last three years, and I cannot recommend it too strongly.

If a new personal computing language were developed from guiding principles, I would hope that it would have much of the flavor of PASCAL. I would hope it would be syntactically uncluttered like PASCAL, not only because it makes the language easier to use, but also because it allows much simpler (smaller) language translators. I would hope it would have control structures at least as strong and as logical as those of PASCAL, and data structuring facilities as simple and powerful as those of PASCAL. It should be designed so that we can write almost all of our software in this one language, including both systems and applications programs. It should not try to provide every feature of every existing language, but rather, like PASCAL, provide a small set of primitive constructs from which users can define their own powerful features. It should allow us to write truly portable programs and to maintain a library of procedures, since a good procedure facility, like that of PASCAL, is perhaps the single most important tool for software developers. But whatever we choose to put in the language, let us design it from principles, and not evolve it from a set of independent features, as was the case with BASIC and FORTRAN.

There are probably several persons out there with thoughts on this subject, and I commend BYTE's Languages Forum as a means of communication. I would also enjoy corresponding directly with anyone with ideas in this area.■

Comments on APL's Characteristics

John E Howland, chairman
Computing and Information Sciences
Trinity University
751 Stadium Dr
San Antonio TX 78284

I would like to add some comments concerning the APL letters published in the November 1977 "Languages Forum." Many of the comments published indicate a lack of familiarity or understanding. This familiarity comes only after extensive use of a programming language. There seems to be a general impression that APL is a relatively new language which has design flaws which are due perhaps to the hasty way in which the language was put together and which are easily corrected by making one or two simple changes. For example, "the APL character set is not ideal for use with 5 by 7 dot matrix printers or video displays," so we should redesign the APL character set. There are already several successful existing 5 by 7 dot matrix implementations of the APL character set; however, the real point here should be that we should consider using a 7 by 9 dot matrix or some other size or hardware technique to implement the APL character set rather than change the character set to fit the hardware.

Another example concerns the order of execution. APL goes from right to left which is clearly backwards, so let's just make one simple change and have it go left to right. One suggestion was that this would be a great help to all those APL programmers who begin entering their programs before they have finished writing them. To me, this is similar to the person who opens his mouth and begins to speak before engaging his brain. The real solution to the suggested problem has nothing to do with the order of evaluation of APL expressions.

Since many readers have only recently encountered APL, some discussion of order of evaluation may be appropriate. Motivation for the APL order of execution can be traced to the standard mathematical way of handling functions of a single argument. In a sequence of functions such as Sin Arctan X, the order of evaluation is Sin of Arctan of X. The value of the entire expression to the right is the argument to a unary function, and this argument is usually

written on the righthand side of the function. The APL language includes a large number of primitive functions. Rather than develop a complicated rule giving priorities of primitive and user defined functions, all such priorities were eliminated. This also allowed user defined functions to be given the same importance and syntax as primitive functions. The rule for evaluating functions of a single argument is extended to functions of two arguments, using infix notation, by having the right argument be the value of the entire expression to the right and the lefthand argument be the first value to the left of the function. A consequence of this extension is that the only nonredundant use of parentheses, to alter the order of evaluation, is to form the left argument of a function.

To summarize, APL order of evaluation from right to left comes from the use of standard function notation of writing the argument of a monadic function on the right of the function and the desire to introduce no hierarchy of evaluation such as multiplication before addition.

If one desires to evaluate expressions from left to right, using no priorities among functions, then one will probably have to introduce a "left monadic" notation such as

X Arctan Sin.

which, unfortunately, has to be read from right to left! If one extends this notation to functions of two arguments in a similar manner, then one has the problem of writing the subtrahend and divisor to the left of the function symbol so that 3 ÷ 6 equals 2. Also, assignments are probably made to the right, rather than the left. Such extensions lead to a confusing notation because they must be read from right to left.

It should be clear at this point that the right to left order of evaluation rule which is used in APL was not chosen in an arbitrary manner. It was chosen so that APL could be read from left to right.

APL is not a new language which was thrown together quickly. Actually, it is one of the oldest computer languages dating back to before 1962. Unlike most computer languages, APL enjoyed an extended period of development and refinement before it was implemented on a computer. During this time, many changes were made. The changes were easy to make because there were no interpreters to change and no user community to complain. The APL character set evolved during this time to its present form. One unusual aspect of this character set is the use of overstrikes to represent some functions. This technique allows easy addition of new characters for new functions when they are incorporated into the APL language.

In summary, the APL language was very carefully designed. Few, if any, arbitrary choices were made during the development of APL. Some of the controversial features, such as the character set and order of evaluation, are based on standard mathematical notation and convention and are not easily changed.■

Warnier-Orr Diagrams: Some Further Thoughts

GT Wedemeyer
#17 Forest View Trlr Ct
Iowa City IA 52240

The article "Structured Program Design" in the October 1977 BYTE, page 146, has certainly simplified my thinking. However, the use of the symbol ⊕ seems to violate a rule implicit in the Warnier-Orr diagram that one need not and in fact must not go up in a list contained within a bracket of a given order. The ⊕ symbol requires checking up and down the list of case statements. I believe that what is meant is illustrated in figure 1. In this example CASE J is equivalent to ROLL = "J." This manner of diagramming clarifies the relationship between statements having alternatives and statements not having alternatives. It also eliminates the need for the instruction SKIP, since the finding of no more items in a list of a given order is the equivalent of an instruction to return to the proper place in the list of the next lower order, where the order of a list is its position from left to right as shown in figure 2.

I would like to define the instruction RETURN to mean "in the list of next lower

Figure 1.

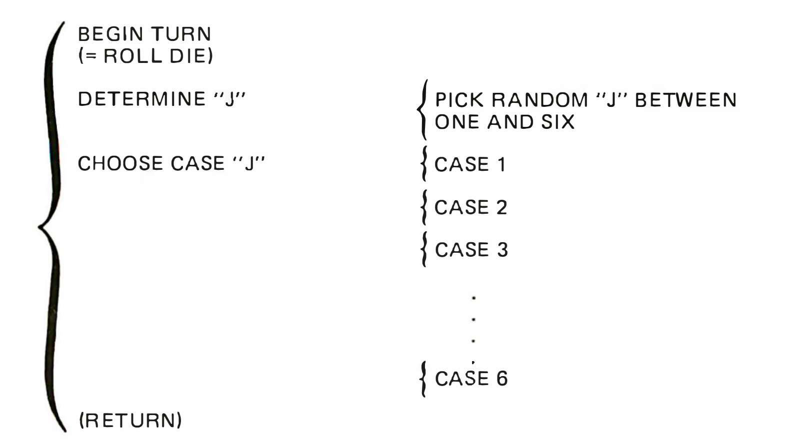
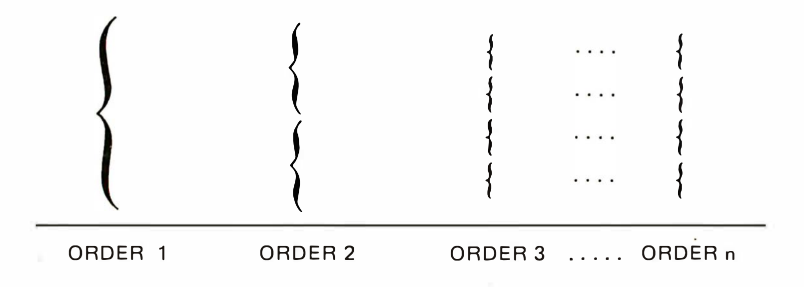


Figure 2.



order than the list in which this instruction is found, complete the step immediately following the lowest completed step." Although this instruction seems implicit, as I indicated above, I would prefer that it be explicitly stated, and I think it would make the diagrams more easily followed.

Dave Higgins replies:

It appears from your letter that you are very interested in using the Warnier-Orr diagramming techniques. I think you will be pleased with the results.

I'd like to comment on the suggestions you made for improving the diagrams. Unlike flowcharts, which have become quite rigid and inflexible in form, the Warnier-Orr diagrams are still in a relative infancy, and do still change occasionally. We here at Langston, Kitch have made some minor modifications to the diagrams in the last year in order to add some capabilities that were previously vague or nonexistent. We are continually evaluating the diagrams, looking for shortcomings or ambiguities, and therefore welcome suggestions along these lines. It is in this light that I considered your suggestions for revising some of the notation.

First of all, with respect to your ideas concerning the representational form of a CASE statement: I think your objection

Listing 1.

```
        .
        .
        .
300 REM   CASE STATEMENT
310 REM     DETERMINE CASE "J"
320 LET J=INT(RND(0)*6+1)
330 ON J GOTO 340,380,420,460,500,540
340 REM     CASE 1
350                 .
     case 1 process
                    .
370 GOTO 570
380 REM     CASE 2
390                 .
     case 2 process
                    .
410 GOTO 570
                    .
     cases 3-6 as above
                    .
                    .
570 REM   END CASE
```

Figure 3.

```
        ⎧ DAY = MONDAY    { ~~~
        ⎪   (0,1)
        ⎪     ⊕
~~~     ⎨ DAY = TUESDAY   { ~~~
        ⎪   (0,1)
        ⎪     ⊕
        ⎩ DAY = WEDNESDAY { ~~~
            (0,1)
```

Listing 2.

```
      .
      .
300 REM   CASE STATEMENT
310 IF D$="MONDAY" THEN 330 ELSE IF D$="TUESDAY" THEN 360
    ELSE IF D$="WEDNESDAY" THEN 400
320 GOTO 440
330 REM   CASE 1: DAY = MONDAY
      .
    monday process
      .
350 GOTO 440
360 REM   CASE 2: DAY = TUESDAY
      .
    tuesday process
      .
390 REM   CASE 3: DAY = WEDNESDAY
      .
    wednesday process
      .
440 REM END CASE
```

to the use of the ⊕ symbol stems from the fact that there are two primary ways to actually code a CASE structure. One way is with the use of a "computed GOTO or GOSUB." The diagram you show is ideally suited for translation into a computed GOTO, which would look something like listing 1. But I don't think this is a worthwhile change to make to the basic form of the diagrams themselves. The reason is this: although your method works fine for CASE statements that lend themselves to computed GOTO's, there are a whole host of other CASE statements where the use of a computed GOTO is an extreme inconvenience. Take, for example, the CASE of figure 3. It would be inconvenient to have to rig up a computed GOTO to execute this CASE. It is much simpler to code it using a "nested IF" statement, which is the other popular way to code CASE statements. In pseudocode, this CASE is:

```
IF DAY = MONDAY
     THEN MONDAY-ROUTINE
ELSE IF DAY = TUESDAY
     THEN TUESDAY-ROUTINE
ELSE IF DAY = WEDNESDAY
     THEN WEDNESDAY-ROUTINE
```

You can see the natural one-to-one correspondence between the Warnier-Orr diagram and the pseudo-code. This is easily translated to code in listing 2. Listing 3 shows an alternative for those BASICs without the nested IF capability. This is the preferred method for coding a case statement because this method will work for *all* CASE statements, regardless of whether or not the CASE is suited for a computed GOTO. Also, with the computed GOTO, you must be sure that your "J" is restricted to the proper range. This is not to say that you can never use the computed GOTO; just be sure that its use is justified and then

```
300 REM   CASE STATEMENT
310 IF D$="MONDAY" THEN 350
320 IF D$="TUESDAY" THEN 400
330 IF D$="WEDNESDAY" THEN 450
340 GOTO 500
350 REM   CASE 1: DAY = MONDAY
            .
      monday process
            .
390 GOTO 500
400 REM   CASE 2: DAY = TUESDAY
            .
      tuesday process
            .
440 GOTO 500
450 REM   CASE 3: DAY = WEDNESDAY
            .
      wednesday process
            .
500 REM END CASE
            .
            .
```

Listing 3.

be very careful. Personally, I feel it is more trouble than it is worth.

As for the elimination of the brackets with "SKIP" in them: I don't believe that you really want to do this. For instance, in the BUG game published in the October 1977 BYTE, no action is taken when a player rolls a "BODY" on the dice but already has a body. This bracket is filled with the notation "SKIP," which indicates that, although the bracket is an essential part of the logic of the diagram, nothing is to be done there. However, in future versions of the game, you might just decide to tell the player that "YOU ALREADY HAVE A BODY" when that condition occurs. If the original diagram is left with the empty brackets intact, you have a fixed and ready place to put that PRINT command. The design is very easy to change and the documentation for the new program is only a matter of erasing one line and replacing it with another.

Also, I don't believe that we need to add the (RETURN) command at the end of the brackets as you suggest. As you state, the return to the next highest level in the diagram is already implied at the end of *each bracket:* therefore adding (RETURN) on each bracket would amount to a lot of "busywork," which would clutter up the diagrams with a lot of unnecessary information.

Again, I'd like to thank you for your suggestions and extend an invitation for all the readers of BYTE to submit their suggestions for improvement of the Warnier-Orr diagrams to either Langston, Kitch and Associates or to me for examination.

Dave Higgins
Langston Kitch and Associates Inc
715 E 8th
Topeka KS 66607
(913) 233-2349■



ON USING AMATEUR RADIO FOR PC NETS

Jeff Steinwedel offers the only feasible solution for CIE Nets, Distributed Communications Network, or whatever you may wish to call it. Amateur radio, because of its disciplined ranks, would be the very ideal place to start. We do not need another uncontrollable "Topsy" that one finds on the Citizen's Band.

Some refined computer work has already begun on the amateur bands. I've just completed an interface board for frequency control, and another for the computer to do all of the log work by filing dates and time of contacts, and even their call signs. Conditions are already open: the allotted VHF frequencies welcome experimentation, within FCC rules, of course.

Jack Chancellor W9SON
4736 Amethyst Rdg
Rockford IL 61102

MORE ON COMPUTER CONTROLLED PROSTHESES

The January 1978 BYTE Letters column contains a letter from Don Baker regarding computer controlled prostheses. I call to his attention the work currently being carried out at Northwestern University's Rehabilitation Engineering Center at the Rehabilitation Institute of Chicago.

Under the direction of Dr Dudley Childress, the Center has developed a multitude of prosthetic devices for the crippled patient. Foremost among these (in my opinion) is the design and construction of prosthetic limbs, namely a "bionic" arm and hand. This device amplifies the myoelectric surface potentials on the skin which are generated by muscle contraction and converts the signals into finger motion through a network of electronic circuitry and electromechanical components. By "thinking" to extend the arm, for example, the patient can open and close the thumb and forefinger on the prosthetic limb. While the grip strength of 25 pounds is nowhere near the ability to crush steel, the patient gains a great deal of freedom in lifestyle than that which he had as an amputee.

Mr Baker suggested a computer controlled wheelchair as a possible solution to mobility problems for the handicapped. Northwestern has already thought of the same thing and has gone on to develop such a machine. It consists of an electric wheelchair fitted with an array of batteries, electronic hardware, and specially designed input and output devices which are in the form of straws. The effectiveness of the device is best seen in abilities of the Rehabilitation Center's receptionist/secretary, who is a quadriplegic. Doubling as a public relations spokesperson as well, she can operate slide shows, telephones, lights, and even type from her seat in the wheelchair via coupling to a microcomputer. Paralyzed from the neck down, she communicates with the computer by sipping and puffing on straws coupled to pressure sensing instruments. Output from the computer is on a video terminal, which is also connected with an electronic typewriter. Through the use of the sipping and puffing mechanisms, and computer supplied "best fit" characters, the typist is able to create words and entire letters on the computer, which are then sent to the typewriter for printing.

At present, the cost of microcomputers limits this complete system to a relatively small segment of the population. Thus, alternate systems have been developed, allowing the user to control eight devices within the home (eg: lights, telephone, toaster, etc). As the cost goes down, we'll be seeing more of these systems in the near future.

With the development of new techniques and mechanisms, the Rehabilitation Engineering Center is enabling more and more crippled patients to face the world more effectively and helping them gain pride in themselves.

Christopher A Kryzan
1012 Waveland Rd
Lake Forest IL 60045

Christopher is president of the Tech Undergraduate Council, Northwestern University Technological Institute.

TROUBLESHOOTING QUERY

I have a BA in photography, but due to a recent car accident my back was injured causing my legs to become partly crippled. Because of this I can no longer work as a photographer, and at present I am repairing calculators for Texas Instruments.

Looking toward the future I have decided to open my own microcomputer repair shop as a new career (with some luck).

Most of the local colleges and training schools offer programming and design theory, but this is not troubleshooting and repair.

Where can I find such a college or training school which offers basic electronic and computer repair? Where can I write to find such information if you don't have it?

Relocating to another state will be no problem, and I'm not concerned with the time required to attain the training.

Larry Bernard
1625 16 St, Apt 255
Lubbock TX 79401

Readers who can answer Mr Bernard's questions are encouraged to correspond with him directly.

A D TO A FROM THE UK

In certain articles of BYTE I have noticed circuits which could, in my opinion, be improved by use of British devices which, for some reason, are not used in American articles.

The best example of this is the Ferranti ZN425E 8 bit digital to analog converter. This device retails for approximately $8 in the UK and, as far as I can tell, is superior to the MC1408L-8. One

advantage is that the ZN425E can be converted to an analog to digital converter with the addition of just two more ICs costing about $3 total.

Also, I think there should be more articles like Ciarcia's Circuit Cellar, since his articles are easily adapted to any microcomputer, rather than being designed for use with any one type. My reason for this bias is that I am designing my own microcomputer.

A K Kenny
43 Simonbarn Av
Fenham, Newcastle upon Tyne
Tyne and Wear NE4 9VA
ENGLAND

Interested readers can contact Ferranti Electric Inc, E Bethpage Rd, Plainview NY 11803.

READING STRINGS

I read with great interest Wayne Ledder's description of how a string of ASCII digits can be read and converted to a binary number in "A Novice's Eye on Computer Arithmetic" (January 1978 BYTE, page 150). A faster, cleaner, and easier algorithm exists for this purpose.

To read a 3 digit number, Ledder recommends placing the first digit (after subtracting ASCII "0") into memory location HUNS, the second into TENS, and the third into UNITS. Then HUNS is multiplied by 100, TENS by 10, and these results are added; UNITS is added to this sum to give the final result. Clearly, this method works. However, it is inconvenient to use for two reasons. First, the program itself must be modified if one wishes to input, say, four digit numbers. Second, the number must be typed using a fixed number of digits. Now, how would you feel if your tiny BASIC made you type things like 00001, or interpreted 0001 either as something ridiculous or an error?

I think there is a better way. The following algorithm is cleaner and as easy to implement.

1. Set NUM to 0.
2. Get a digit from input. If it is not a digit (eg: a blank or a new line), terminate.
3. Otherwise, convert the digit from ASCII by subtracting the code for ASCII "0" from it.
4. Multiply NUM by 10. Then add the digit to it.
5. Go to step 2.

When the algorithm terminates, the value of NUM will be the binary number corresponding to the ASCII coded input.

Several comments are in order. First, the multiplication in step 4 can be performed quickly by adding the value of NUM shifted left three times to the value of NUM shifted left once. Second, the processing of the first digit should probably be moved outside of the loop. This facilitates checking for a negative sign, avoids an unnecessary multiplication in step 4 on the first iteration, and makes it possible to check for a completely blank line (which should be treated as an error, not as zero).

This algorithm requires no leading zeroes and works for numbers of any length. It is also quite fast; in reading number less than 65,536, it requires only 3 n 16 bit shifts and 2 n 16 bit adds, to read an n digit number. Unfortunately, I can claim no credit for it since it has been in existence for many years.

Eric Hamilton
Dunster D-11
Harvard University
Cambridge MA 02138

DEMISE OF MAPLE

Sad to report, *MicroAPL Enthusiasts* has gone to seed. The major cause of its demise has been a severe deficiency in creative literary sap. When we started this seedling, we'd hoped for a forum which would someday branch to many interesting discussions on that most fascinating of languages: APL. Since then, although the response has been good, the literary stuff has been flowing in at the rate of frozen maple syrup. As the instigators of all this, we found ourselves unable to gather enough material to form the critical mass needed to get the chain reaction of ideas started. Therefore, we have decided to discorporate, and return MAPLE to virtual memory storage in that bit bucket in the sky.

R Low
J Sikorski
POB 574 NUMS
Chicago IL 60611

HUMAN FACTORS ENGINEERING NEEDED?

Today I discovered that nobody really cares about us, at least those of us who use computer terminals day after day.

I was doing a data base search through the INSPEC files looking for information about "the office of the future." Most searches that were performed were quite successful (giving up to 160 references). However, a combined search on display devices and human factors found one entry (on digital watches). Even less rewarding was a search on data acquisition and human factors—no references. I can only assume that no one cares about the user.

At the Canadian Computer Show in Toronto in November, my sister and I ran a quick informal survey of keyboards of computer terminals. Typically, the keyboards could not have been designed with any user in mind. Problems of ugly color schemes; glare on the keys from overhead lighting, lack of "feel"

in the keyboard, beeps (often not adjustable) to replace tactile feedback, and soft keying (instead of a bouncy switch), lack of position adjustment of the keyboard, and lack of an armrest in front of the keys were problems that we frequently noted. Only about two or three keyboards came anywhere near being reasonably pleasant to use. Human factors appear to have been ignored by almost all manufacturers.

Hopefully in the future we can have some articles about human factors in the terminal device design. For too long the industry has pushed human factors in man-machine dialog software and ignored the hardware.

Dr John C McCallum, Assistant Professor
Dept of Computer Science
York University
4700 Keele St
Downsview Ontario M3J 1P3
CANADA

MEDICAL AND DENTAL SOFTWARE NEEDED

A recent copy of *Time* magazine referred briefly to a successful US application of microcomputers to the basic requirements of individual doctors and dentists.

If you or any of your readers happen to know of the firm(s) responsible for this application I would be most grateful to learn their address(es).

Philip D Burke
GPO Box 498
Adelaide S AUSTRALIA 5001

ANOTHER LETTER RECEIVED WITH A COMPLETED READER SURVEY FORM

Miscellaneous comments apropos personal computer usage:

The languages available are atrocious. The few good languages are not available on personal systems. Languages I consider good, even if not practical on a micro, are: APL, PASCAL, ALGOL 68, MODULA (yes, I've seen examples of MODULA), in no particular order. Each has some good and some bad features. What we need is a synthesis.

I keep hearing about "high level language machines." In my opinion, they are long overdue. Where are they? Where, at least, is the computer that can *efficiently* run an intermediate language interpreter, at a price I can afford? What I need is an HP-3000 microcomputer, I guess.

Where languages are concerned, I suppose that a good systems implementation language is most needed, although why do so few people seem to recognize this obvious fact? Think how it would simplify developing operating systems and Star Trek games that are identical on *all* computers they run on. Is that bad?

I want to have fun and learn things with my computer. To me, fun is writing aesthetically pleasing and correct programs. That's hard to do in BASIC.

CLH

RECEIVED FROM A RESPONDENT TO BYTE'S 1978 READER SURVEY

I would like to offer some additional comments which you may find useful in your survey. I fully intend to purchase a personal computer system in the very near future. The equipment and approximate prices I intend to pay are detailed in the survey. The major factors influencing this purchase are as follows:

- The availability or near availability of a high level block structured language compiler (C, PASCAL or ALGOL).
- The vendor's financial stability.
- The availability and compatibility of peripheral equipment.
- The availability of a simple, powerful monitor or operating system.

I will purchase a prebuilt system and have very little interest in assembly or hardware fiddling. I also have very little interest in assembly language coding and will use the home computer to develop projects in the area of artificial intelligence.

Anonymous

COMPUTER CHESS

I am told by John M Lusa of Infosystems that your magazine specializes in small systems.

I wonder if you know of a computer that plays chess at the master level. I am very desirous of owning such a product and I would truly appreciate it if you could in any way lead me to it.

Philip Restagno
2910 De Witt Pl
Bronx NY 10469

Playing chess at a master level is one of artificial intelligence's perenial projects. As of now, the closest you can come is an expensive laboratory project executed on a large computer of conventional design. But this is hardly a commerical product available at your local computer store.

MATSUSHITA MYSTERY PROCESSOR

Recently I came across a Matsushita MN5763 microprocessor, and have been unable to find any information about it. Could you or a reader tell me anything about this part or about where I can obtain information on it?

Jeff Spoelstra
7405 Palm Dr
Urbandale IA 50322

BYTE's Bits

Electronic Music Workshops at New England Conservatory

The New England Conservatory of Music will hold a Summer School June 26 thru August 4 1978, featuring workshops, courses and master classes. Highlights will be the Electronic Music Workshop, June 26 thru June 30 with Robert Ceely, and the Electronic Music in the Classroom Workshop, July 10 thru July 14 with Larry Allen.

The Electronic Music Workshop with Robert Ceely will be divided into two parts. Part A will be a lecture demonstration of the hardware and software of electronic music. Part B will give students hands-on experience with various synthesizers.

Electronic Music in the Classroom with Larry Allen will be an exploration for the classroom music educator of the goals, outlines, lesson plans, and electronic equipment to be used in developing a comprehensive junior high, senior high, college or adult education music curriculum.■

Instruction Search

Have you ever found yourself executing as instructions information you intended as data, only to get garbage? Sure you have; we all do this at one time or another.

One day, while interacting with my KIM-1, I found myself executing a hexadecimal 27 which I had accidentally left in a location. It multiplied another number by two and added one. Upon closer inspection, I found hexadecimal 27 to be a previously undefined rotate one bit left instruction, a very powerful instruction. Including my new instruction, there are now 147 instructions defined for the 6502 processor, out of 256 possible in the range from hexadecimal 00 to FF. That leaves 119 instructions undefined. The problem is finding them.

I am inclined to believe the best way to determine the difference between garbage and a valid instruction is to continue programming in a normal fashion and when an error is made and I find myself executing an undefined instruction, follow it through. This instruction search is not limited to the 6502; it applies to every processor on the market. Indeed, the store zero instruction on the IBM 7090 was found in a similar fashion at a time when that macrocomputer was at a stage similar to that of the present microcomputer.

I do not advocate sloppy programming. It should be advoided at all costs. However, when a mistake is made and a result is obtained, it should be studied. Something of value may be found.

Francis J O'Reilly
42 Markwood Rd
Ardsley NY 10502■

A Quick Wire Unwrapping Tool. . .

Unwrapping wires from posts on circuit boards is a simple task with the correct tool. Commercial unwrapping tools are usually not practical for the person having only an occasional need, so improvised methods are in order. One such method was described on page 17 of the December 1975 BYTE. I found that method took more time than I wanted to spend on these jobs.

A simple tool that can be made in a few minutes meets the requirements of being cheap, easy to use, made from readily available material. It does not damage the posts and removes the wire rapidly. All you need is a small diameter metal (brass if you are concerned about damage to the posts) tube that fits closely over the posts. Such tubing is often available in brass at hobby shops. To make it into an unwrapping tool, simply file a notch across the side and end of the tube to a depth about twice the diameter of the wire to be removed. To preserve the strength of the fitted end of the tube, file the notch into about 1/3 the diameter of the tube. If you have a fine file or other tool, cut a small nick into the side of the notch. This enables it to hook onto the wire, which will then be removed from the post when it is unwrapped and the tool is removed.

Ready sources of tubes (including handle) are mechanical pencils and ballpoint pens. The mechanical pencil is best and easiest to "build" into the desired tool. To convert ballpoint pens into unwrapping tools, it is of course necessary to remove the ballpoint and ink. It will also probably be necessary to drill the tube to a size that will fit over the wire wrap posts.

Donald C Weber
1201 Inwood Ter
Jacksonville FL 32207■

Component Types and Values

Unless otherwise noted, all components and values in the schematics of BYTE magazine are assumed to be typical of low power logic and signal electronics:

Resistors: Power ratings of ¼ W, carbon composition, 10% tolerance or 5% tolerance depending on value are standard default assumptions. Values are in ohms (no units symbol), decimal thousands of ohms (K units symbol), decimal millions of ohms (M units symbol). Typical exceptions to these defaults are:

> 10 W, ½ W are notations of typical power ratings differing from ¼ W.
>
> 1% is a notation of an explicit resistance value tolerance when 10% is not adequate.

Capacitors: Capacitors are assumed to be 20% tolerance, nonpolarized, with voltage ratings greater than or equal to the difference between the most positive power supply voltage and the most negative power supply voltage. Values are in microfarads (no units symbol, or units symbol μF or μF) or picofarads (units symbol pF). Typical exceptions to these defaults are:

> Electrolytic capacitors are indicated by explicit notation of polarities (+) and (−) on the diagram.
>
> Explicitly noted voltage ratings always appear for electrolytics, and occasionally for other types.
>
> Where some other tolerance parameter is critical (such as temperature coefficient, type of capacitor technology, etc) it will be noted near the part in question.

Power Supply Circuits: Power distribution circuits are assumed to follow good engineering practices for prototype equipment: heavy distribution bus conductors, frequent bypass capacitors (.01 to .5 μF ceramic disk) spread throughout the board in question, and at least one fairly large (eg: 5 to 25 μF) electrolytic bypass capacitor per supply voltage per board. Bypass capacitors are wired from the supply voltage to ground. These assumptions are not noted in each drawing, but should be observed as a matter of course.■

New Product Information

Lucas-Adams Labs UnLtd is proud to announce the perfection of the following special function boards, all plug-in compatible with Altair (S-100) bus mainframes, and adaptable for other buses with a transfer:

Mainframe expander board — hydraulic: Two 2 cm hydraulic jacks extend to a maximum of 14 cm to expand the available internal space of most ductile mainframes. Complete with integral fluid reservoirs and high capacity pump.

Freon cycle refrigerator board with multiple radiator boards: Eliminate the noisy mechanical fan and keep your micro's temperature down with this quiet running refrigerator board. Compressor runs off the mainframe's +8 V supply; usable with up to 12 radiator boards, each to be located near a memory or processor board to keep it cool.

Solar energy package board: For an ecologically sound second power source, try our solar energy board. Fitting into a single Altair (S-100) bus slot, an extender on top of the board unfolds, software controlled, to expose a 12 foot square solar panel, with ample capacity for your entire bus during the daylight hours.

Hydroelectric power board: This clean source of power is generated by a diversion of the source to drain flow of 10^{12} FETs contained in only 64 LSI chips. High tension printed circuit lines transfer power to an on board substation for use on the bus.

Garbage compactor board: Bothered by garbage from old programs, obsolete data, initialization? Our garbage compactor board compresses the equivalent of a full 64 K of garbage into the space of only one 4 K static or dynamic memory board, for easy disposal.

Terminal board: This board is sold with only two days life left of declining service, at which point it self-destructs. Nonrepairable.

DART random number board: On the board are four concentric shift register rings and 16 pointed, feathered electrodes for truly random number generation.

PROM memories board: Complete with a big band clocking and rhythm section, this board boasts a hardwood dance floor option and fast access time. Refresh area on board (for volatile spirits only).

Abacus board: This nonvolatile processor can provide emergency computing ability during complete power failure. Comes with on board direct access BEAD memory. (User must provide some logic.)■

BYTE's Bugs

A Note About Simulations, Part 3

I have just received a letter from David O'Neil of Greenacres FL pointing out some errors in the program which accompanied my article "Simulation of Motion Part 3" in the January 1978 BYTE. According to Dave, lines 680 and 970 should be changed as follows:

```
680 LET A=(COS(G)*D*V2+
         COS(L)*F)/M
970 DATA 1.6,5.6,0.0337,1.0E-4,1.7,
         0.0,0.0333,1.0E-4,100,0.0,
         0.0333,1.0E-4
```

Line 330 is incorrect and should be deleted; and lines 490, 510 and 550 are superflous and may be deleted. I agree in all cases and apologize for my poor proofreading.■

Stephen P Smith
POB 841
Parksley VA 23421

That's the Way the Paper Folds

I would like to call to your attention an error noticed on the cover of the December 1977 BYTE.

The paper coming out of the printer has a very unusual fold; it is not the normal fan fold. In fact it is difficult to see how the paper is fed with *that* fold pattern (unless on a roll).

Other than the "ancient technology" of paper folding, I enjoyed the article on the Star Trek computers.■

Richard L McCracken
85 E Emerson
Chula Vista CA 92011

There is no obvious supply of paper, either. But the idea is conveyed, and even if we could, we're not about to revoke Robert Tinney's artistic license.

Address Correction

In Sol Libes' article "Where to Get Bargains in Used Computer Equipment" which appeared in the December 1977 BYTE on page 154, the entry for the Rondure Co was incorrectly stated. The current address of that company is:

Rondure Co
2522 Butler St
Dallas TX 75235

Thanks to Stan Shannon, president of Rondure, for pointing out this error.■

Chess and Computers

____**Chess and Computers** by David Levy. If you enjoy playing chess, then you should thoroughly enjoy **Chess and Computers.** This 145 page paperbound book is loaded with chess games played by computers. The games are computer versus computer and computer versus human. When you settle down with this book, it would be a good idea to set up your chess board and play the games. As with any good chess book, half the enjoyment is found in playing along, duplicating the moves, reading the comments by the author and adding your own comments. $8.95.



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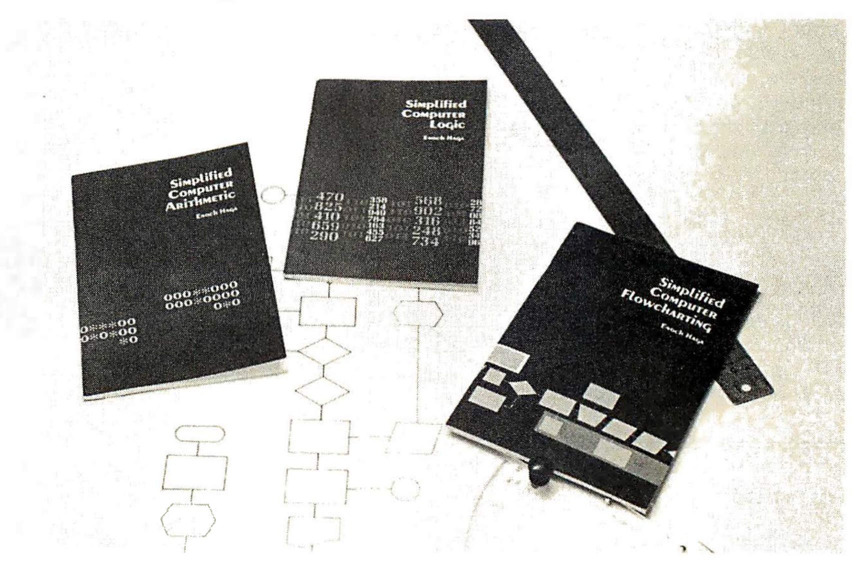
____**Dr Dobb's Journal of Computer Calisthenics and Orthodontia Volume I** is a collection of everything from the first year of Jim Warren's outstanding journal. As Carl Helmers, Editor in Chief of BYTE Magazine says, "Dr Dobb's Journal can help make your computer an indentured servant." $13.00.

____**Assembly Level Programming for Small Computers** by Walter H Weller. One of the most professionally produced books we've seen. From front cover to back, this book is clear, detailed, and beautifully produced. Using a pseudo mnemonic assembly language, Walter Weller takes you inside the whys and hows of table referencing, data stacks, number conversions, floating point arithmetic, and much, much more. Surely one of the most complete books on this topic. **Assembly Level Programming for Small Computers** is a must for the serious small systems user. $14.95 hardcover.

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____**The Compulator Book** by R P Haviland. Tells you how to mate the computer with the calculator. This unique new volume provides ideas, design information and/or printed circuit boards for calculator chip projects including computer interface for log and trig functions, electronic lock, dial a telephone, interface to Teletype, tape control of calculator, giant displays, store and display, and many more. Yours for $7.95.

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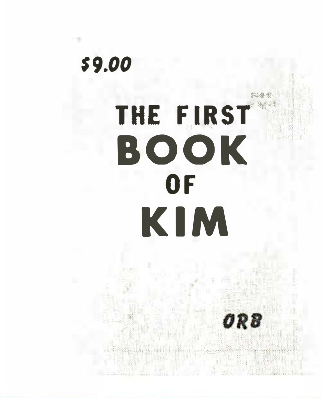
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____**The Linear And Control Circuits Handbook** is the latest offering in the Texas Instruments series. Roboticists and others interested in linear and analog control circuitry will find much of interest here. Devices covered include op amps, timers, voltage comparators, analog switches, and voltage regulators.

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____**The First Book of KIM.** Attention KIM users! Here is the book you've been waiting for. In it you'll find a beginner's guide to the MOS Technology KIM-1 microcomputer as well as an assortment of games including Card Dealer, Chess Clock, Horse Race, Lunar Lander and Music Box. Also featured are diagnostic and utility programs for testing both the computer and external equipment (such as cassette recorders), and chapters on expanding memory and controlling analog devices. This 176 page volume should prove an essential addition to any KIM user's library. $9.00.

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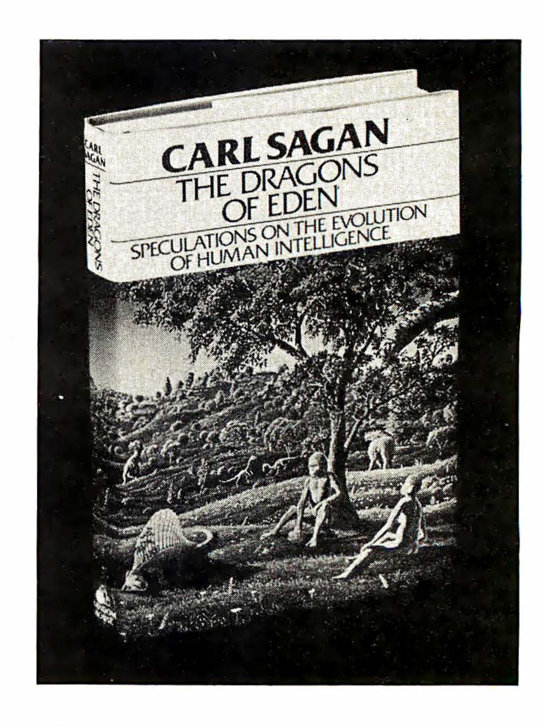
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Book Reviews

The Dragons of Eden
by Carl Sagan
Random House, New York
263 pages, 6½ by 9½ inches
$8.95

Carl Sagan's premise is that the human brain is a very highly developed general purpose biological computer. *Dragons of Eden* traces the evolution of this machine from its most primitive beginnings. The provocative title stems from the interesting theory that the early reptilian (hence dragon) brain is still very active in humans as a subcomponent of our full mental equipment. The theory that brain evolution occurred not so much by change as by accretion of new components seems to be substantiated both by physiology and by function. Sagan suggests that occasional apparent subversion of higher brain functions by the "dragonian" sub-brain may be the true referent of various Eden mythological allegories.

Later chapters of the book deal with brain functioning and potential for development. A most interesting aspect of this is that the left and right hemispheres of the brain appear to function with a high degree of independence, although they are closely interconnected in the normal brain. One hemisphere seems to operate principally in a "digital" mode, dealing with analytical

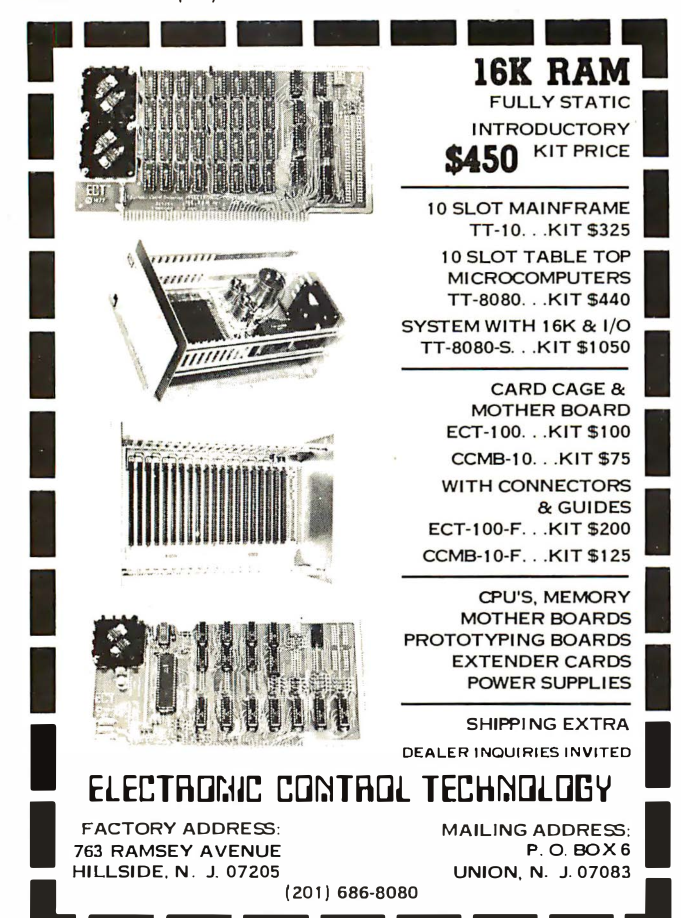


computations, while the other simulates more "analog" qualities, and is the seat of such nebulous functions as inspiration and intuition.

In his discussions of the computer, for comparision of the brain to an artificially evolved intelligence that is more completely understood, Sagan includes the following observations (page 216):

> *The two games, Pong and Space War, suggest a gradual elaboration of computer graphics so that we gain an experiential and intuitive understanding of the laws of physics. The laws of physics are almost always stated in analytical and algebraic—that is to say, left-hemisphere—terms; for example, Newton's second law is written $F = m\ a$, and the inverse square law of gravitation as $F = G\ M\ m/r^2$. These analytical representations are extremely useful, and it is certainly interesting that the universe is made in such a way that the motion of objects can be described by such relatively simple laws. But these laws are nothing more than abstractions from experience. Fundamentally they are mnemonic devices. They permit us to remember in a simple way a great range of cases that would individually be much more difficult to remember—at least in the sense of memory as understood by the left hemisphere. Computer graphics give the prospective physical or biological scientist a wide range of experience with the cases his laws of nature summarize; but its most important function may be to permit those who are not scientists to grasp in an intuitive but nevertheless deep manner what the laws of nature are about.*

Benefits to be derived by the computer enthusiast from the understanding of the functioning of the human brain presented in this book are twofold: it offers new understanding of the way biological intelligences function which may be of value in developing computer systems, and it suggests ways in which computers may be used to augment and stimulate the biological mind. Sagan submits that the computer itself may logically be considered to be the next step in human brain evolution, the mind having by its own ability finally released itself from



restriction to a purely biological mechanism.

Dragons of Eden well deserves its high place on the nation's nonfiction best-seller lists, and should be read with relish by anyone with an interest in the mechanics of intelligence, whether natural or artificial.

Jim Heter
107½ S Carondelet St
Los Angeles CA 90057■

Digital Computer Electronics
by Albert Paul Malvino
McGraw-Hill, New York 1977
393 pages
$14.95

"If the action of small computers is not quite clear, if you feel something is blocking your understanding of microprocessors, or if the whole computer thing has never quite come together, then this is the book you've been waiting for." Thus, author Malvino describes the audience for whom this book was written. And, although it is a text for technicians, the author presents the material in such a clear, readable style that the book is an invaluable reference for anyone wishing to improve his/her understanding of computers in general and microcomputers in particular.

Prerequisites to understanding the book are electronics to the level of DC and AC theory, with transistors and diodes.

The first seven chapters are devoted to the basic logic circuits, binary numbers and arithmetic circuits. Explanations of logic circuits, flip flops, registers and memories make the book worth the price for these topics alone.

Most computer books present a block diagram of a "typical" computer and use that as the frame of reference for the rest of the book. Dr Malvino has designed a working 8 bit computer with only six instructions in its instruction set. He calls it SAP-1 (for simple as possible, #1). He uses SAP-1 to explain how the basic elements of a computer are tied together into a working system. Anyone with an understanding of TTL could build a SAP-1 computer if desired. SAP-1 is used to explain such concepts as busing, three state logic, elementary programming, instruction fetch cycle, instruction execution cycle, and operation of the internal control unit.

In chapter 9, the author explains the significance of adding jump instructions to the instruction set of a computer, and proceeds to design SAP-2, a 12 bit working computer with 28 instructions in its instruction set, including six jump instructions.

Chapters 10, 11 and 12 cover advanced

concepts of computers. In chapter 10, the author presents SAP-3, a computer with most of the characteristics of modern computers. Chapters 11 and 12 cover such topics as microprograms, microroutines, variable machine cycles, manual loading, bootstrap loading and fixed point, floating point, and double precision arithemetic.

Although the book is organized as an orderly progression from the basics of logic circuits through advanced computer concepts, each chapter could almost stand alone as a comprehensive treatment of its topic. For example, if you already understand the type D flip flop, then you would have no trouble in understanding chapter 6 on registers.

If you are associated with computers from a purely hobbyist viewpoint, with little or no interest in the technical "innards," then this book is not for you. However, if you hope to learn enough to troubleshoot your own, then this book will surely prove helpful. If you have a strong technical interest in computers, whether as a hobbyist or a technician, then you need a copy of this book.

Dr Tom Lukers
Rt 1 Box 277B
Lufkin TX 75901■

The Elements of Programming Style
by B W Kernighan and P J Plauger
McGraw-Hill, New York 1974
147 pages paperback
$2.65

This book should be in the library of every computer enthusiast, for it bridges the awful gap between those beginning moments, and clean, efficient code. By teaching sound principles, the authors give the reader a definite method for improving skills in programming. There is a need for programmers to proofread their code with a copy editor's blue pencil. Yet few of us know how. The old adage prevails: "If it works, leave it alone." This bromide is a carte blanche for programmers of every level of skill to leave confusing code alone, since most programs are judged by the result, and not by the means. Yet in the microcomputer business, it is critical that space be well used.

To their everlasting credit, the authors' first lesson is, in my opinion, the most important. It requires clarity of expression. Make the code show what it does, don't hide the purpose in elegant expressions. Nothing is more frustrating than to attempt to figure out the meaning of mysterious code. A programmer must keep in mind that somewhere in the future it may be

necessary to modify the program. That is hard to do when the existing code cannot be deciphered by anyone, including the originator. In every computer center, there are gobs of temporary programs drafted into continued use for years.

To illustrate the principles of good code, the authors use excerpts of actual programs. For any example, the flaws are pointed out, the segment is rewritten, and the general rule is stated. Several points may be discussed for each example. FORTRAN and PL/I are used as model languages, since each is in common usage. Also, familiarity with one language implies that the other can be understood. However, the rules discussed apply in any language, including BASIC and assembler.

The models used are taken from beginning textbooks, where code is usually first seen by the neophyte. One would think that good style would abound in textbooks, but it's just not true. With the authors' help, the reader can read other programmers' code filtered through a solid foundation of principles.

There are lessons in structure, design of input and output and how to format code for clarity. There is an excellent chapter on documentation, my personal curse. Do your variable names mean something? They should carry the mnemonic image of what they represent. Is your code modularized? Do you use comments, or worse yet, overuse them? The recurring theme in this splendid book is to plan your work to be simply stated and executed.

The models used provide a spectrum of programming applications. Some of the examples require a bit of higher math to follow, but the lesson is very clear. There are models dealing with student grades, salesmen's tallies, and sorting. There is meat here, for both the novice and professional.

In citing the textbooks from which they drew examples, the authors provide a list of manuals of instruction for the reader. There is a somewhat brief section on supplementary reading, as well as a thorough index. There is a summary of rules, which condenses the lessons of the text. Each chapter has a few questions which will allow you to apply the points discussed. It would be a bargain at a much higher price than the modest $2.65. This is a valuable book, and I'm glad it is on my shelf.

Noel K Julkowski
Naval Environmental
Prediction Research Facility
Monterey CA 93940■

Languages Forum

Standardization of High Level Languages: Some Questions

E M Greene
5067 Bluestem Dr
Colorado Springs CO 80917

Glen A Taylor proposes standardizing a high level language for personal computing (Languages Forum, November 1977 BYTE, page 190). The proposal has merit, but there are several factors to consider before initiating a standards activity.

1. *What is to be standardized?*

The existing standards for the COBOL, FORTRAN, PL/I, BASIC and MUMPS languages were developed starting from definitions which existed when their respective standardization activities were initiated. There was experience in using and implementing the languages prior to and during the standardization process. The point is that historically standards organizations have *not* been defining *new* languages, but instead have only been refining a definition of an existing language.

Perhaps Mr Taylor had in mind the standardization of an existing language such as APL, PASCAL, or one of the string processing languages. All other "major" languages have standards in existence and organizations responsible for continuing support.

If Mr Taylor had in mind the definition of a subset of an existing language, it should be noted that ANSI has committees actively engaged in preparing standards for subsets of PL/I and COBOL. American National Standard Institute (ANSI) publication X3.10-1966 contains a FORTRAN subset definition. The COBOL standards define a modular approach to implementing COBOL compilers.



2. *Will there be sufficient interest to support a standardization activity?*

The preparation of a standard is a lengthy, technically complex and expensive process. There cannot be a standardization activity without a firm commitment on the part of individuals and organizations to provide continuing support. In addition to the initial development of a standard, consideration has to be given to the continuing support required to maintain an active standard.

3. *Is a standardization activity premature?*

A standard formalizes things "as they are" and assumes a stable environment. The personal computing environment is anything but stable considering the rapidly changing state of the art of small computers. Would a standardization activity be able to accurately predict the personal computing environment far enough into the future to prevent producing a standard which would be obsolete before it is adopted?

4. *How would compliance with a standard be obtained?*

Compliance with standards in the United States is voluntary unless compliance is required by law, regulation, directive or contract. A language standard for personal computing may not be effective unless the vendors can be induced to comply.

5. *Is there a need for a language tailored to personal computing?*

The impetus for a personal computing high level language seems to arise from the concern with the "size" of the existing "large computer" languages. This emphasis is misdirected in that it ignores the history of digital computing: specifically, "small" computers are getting functionally larger as hardware costs continue dropping rapidly, and the existing standard languages, especially FORTRAN, were developed in relatively ancient times when the "large" computers didn't have much more capacity than present day "small" computers. Compilers have been successfully developed which support a substantial subset of PL/I and operate in a 16 K byte computer supported by a single drive floppy disk.

Programming languages are standardized to promote hardware independence, commonality and transportability of programs. Definition of a special language for small computers would go counter to the standardization objectives by creating a barrier

to developing programs on one size computer and using them on a computer of another size. Organizations and persons involved in programming computers of various sizes are not going to be enthusiastic about dissimilar languages for different sizes of computers. If a language for personal computing is not significantly different from existing standard languages, then the effort required to produce a standard would not be justified.■

Grappling with GRAPL: Some Choice Comments

Andrew Koenig
401 Route 22 #46E
North Plainfield NJ 07060

I would like to comment on some of the points that William Leler made in his article ("GRAPLing with APL," November 1977 BYTE, page 220). In particular, most of his objections to the language were really objections to particular implementations, and these should really be much better distinguished.

His first objection is that "all arrays in APL must be homogeneous" and then he goes on to explain that this means that all elements must be of the same "type." I don't know which "type" he means here. Does he mean that they must all be either numeric or character in form? If so, such an objection is hardly adequate, because permitting some elements of an array to be characters while others are numbers complicates substantially the problem of defining the actions of the various functions that make up the language. If, instead, he means that one cannot mix "integer" and "floating-point" values in a single array (an interpretation of his remark which is rendered possible by his use of the phrase "data type" to mean just that in a subsequent paragraph describing GRAPL), then his criticism has nothing to do with the *language*, which defines no distinctions between integers, bits, real numbers, and so on. APL values are numbers or characters, and that's the extent of its type distinctions. (For one approach to the problem of homogeneous versus heterogeneous arrays in APL, see "General Arrays, Operators and Functions" by Ziad Ghandour and Jorge Mezei, in the July 1973 *IBM Journal of Research and Development*.)

His next objection is that there are no constructs for serial operations. This is a minor problem, since conditional branches and recursion are both available: more than that might be nice, but hardly necessary. His comment about "much wasted computation" presumably comes from expressions like:

```
(X=' ')ι0
```

to find the first nonblank string in X; if he objects to the fact that all elements of X are tested for equality to blank, this objection is to an implementation shortcoming, not to a language shortcoming. Idioms of this sort can easily be recognized by an appropriate optimizing compiler, and much of the delight of using APL is in the fact that it frees the programmer from worrying about coding drudgery of this sort.

His third objection is that "APL is terrible for dataset management." This is a void objection, because the concept of a "data set" or "file" is not defined in APL at all. Instead, there is a "shared variable" facility, which is explicitly designed to permit APL programs to communicate with other programs, presumably written in some other language. This definition leaves the particular operations to be implemented as defined by the host environment, and suitable auxiliary processors can make all the data management facilities of a particular environment available to the APL programmer. A failure to make a desired facility available must again be classed as an implementation objection.

His next objection is to APL's lack of interrupt handling. This is an acknowledged problem with the language as currently defined, and he will probably not have long to wait for a reasonable solution.

His next objection is to APL's use of storage space. Surely this is only an implementation objection! In fact, in most APL systems I have used, it is possible to get much more work done in a given amount of space in APL than in FORTRAN, because APL programs take up much less space than their FORTRAN counterparts.

His next objection is that "almost no translation can be performed on APL code." This is simply not true. In particular, neither of the two APL implementations I have worked with require any symbol table lookups while a program is being executed (unless it uses the "execute" function).

His last objection is to APL's lack of character handling. Lack character handling it may, but it is certainly better than many other languages in that regard. See the

aforementioned paper for a big possible improvement.

Now some questions about William Leler's claims for GRAPL:

1) If GRAPL executes left to right, what about assignment? If I want to assign the sum of B and C to A, am I going to have to write A←(B+C) or will the parentheses be unnecessary? If they are unnecessary, the language cannot also have both strict left to right execution and equal function precedences. One reason APL is right to left is that that permits both polynomials and continued fractions to be written without any parentheses at all. Can GRAPL claim a similar advantage?

2) "GRAPL is block structured like ALGOL, which allows a simple and efficient storage management scheme." What is there about APL's block structure that requires complicated or inefficient storage management?

3) What is a KEIL structure?

4) "When a program is executed, it is partially compiled and then executed interpretively. This is one of the fastest methods of execution." This sounds a whole lot like the way IBM's APL systems handle program execution.

5) Are spaces really ignored in GRAPL programs? In other words, is

```
SQRT 2
```

the same as

```
SQRT2
```

? If so, how do you write function SQRT with argument 2?

```
SQRT(2)
```

? If this is the case, you seem not to have gained much; in fact you have lost some consistency by giving primitive functions a different syntax from user defined ones.

Hewlett-Packard now has a (large) minicomputer available with APL microcode. IBM has APL microcode for some 370 models. Can a personal APL system be far behind? (A Canadian company, last I heard, was selling complete APL machines for less than $5000.)

I am becoming increasingly convinced that people who say "here are a few things I don't like about this language; let's design a new one" are barking up the wrong tree: I think there's a good deal more to be learned about compiler design right now than about language design!■

Programming Quickies

Randy G Soderstrom
4601 Goldfinch Dr
Madison WI 53714

Line Combinations

One of the first programs I wrote for my Altair 8800 and TVT-1 system was one which demonstrates the problem of the printed line.

Suppose you have a printer that continuously prints line after line of characters, automatically changing the rightmost character each time. For example, it could start with "a a a a a" followed by "a a a a b," "a a a a c," and so on. When column 1 becomes *a* again, column 2 becomes *b* much like the odometer in your car.

Eventually, every possible combination of letters will be printed out. Most will be meaningless, but among them will be every

Listing 1: Source listing for an 8080-based system with a video output. The program may have to output a carriage return for some video displays.

0	LXI H	041	;Point to
1	040	040	;text line in
2	AAA	AAA	;memory
3	MVI E	036	;Initialize line
4	300	300	;to ASCII @
5	DCR L	055	;sign
6	MOV M,E	163	
7	JNZ	302	
10	005	005	
11	BBB	BBB	
12	DCR L	055	
13	INR L	054	
14	MOV A,M	176	;Get character from memory
15	INR A	074	;Increment it
16	ORI	366	;Make sure it's still
17	300	300	;an ASCII character
20	MOV M,A	167	;Then put it back
21	CPI	376	;If this one flipped over to
22	300	300	;an @ sign; increment
23	JZ	312	;next character
24	013	013	
25	BBB	BBB	
26	MVI L	056	;Else reset pointer to
27	000	000	;start of line
30	IN	333	;Do you want
31	377	377	;to write
32	RAL	027	;out this
33	CC	334	;line?
34	041	041	
35	BBB	BBB	
36	JMP	303	;Start over
37	014	014	
40	BBB	BBB	
41	MVI L	056	;Line output
42	040	040	;routine
43	DCR L	055	
44	MOV A,M	176	
45	Cal	315	,Call output
46	XXX	XXX	;routine
47	YYY	YYY	
50	DCR L	055	;Are we at end
51	INR L	054	;of the line?
52	JNZ	302	;If not, get next
53	043	043	;character.
54	BBB	BBB	
55	Ret	311	;If so, return

AAA Page of character string
BBB Page of program
YYY:XXX: Address of output subroutine

line of next month's BYTE and every line from every book that ever has or ever will be written. All you have to do is look through the printer output and pick out the good pieces.

But wait a minute: just how many different lines are there? On my TVT-1 there are 64 characters and 32 characters per line. This means there are approximately 6×10^{57} different lines. It would take your microprocessor many times the age of the universe to generate them all! [*If your microprocessor produces 50 lines per second, it will take about* 4×10^{48} *years*. . .RC]

You can have some fun generating and displaying a few of them on your video output. In this program, the computer displays only the current line when sense switch 15 is raised. When SS15 is lowered, the machine keeps grinding out new lines, but does not write them out. This is obviously much faster.

Note that, since my television typewriter scrolls automatically at the end of the line, no carriage return is sent. If your line length is different or you use a Teletype, you will have to make suitable modifications. See the end of listing 1 for address explanation.■



Continued from page 46

system currently being distributed include the following:

- *Single user operating system.*
- *PASCAL Compiler.* Standard PASCAL plus extensions for strings, disk files, graphics, system programming (business oriented extensions are planned).
- *Editors.* High performance screen oriented editor for program development and word processing, line oriented editor for hard copy devices.
- *File Manager.* General purpose utility for maintaining a library of disk files (usually floppy disks).
- *Debugger.* Single statement and breakpoint processing, access to program variables.
- *Utilities.* Programs for printing, communicating, accessing disks written under DEC's RT11 system, diagnosing disk faults, desk calculator, etc...
- *BASIC language compiler.* Implemented for those who insist on using BASIC, but may wish to write powerful subroutines in PASCAL. (The compiler works, but subroutine binding is not yet ready.)

Major components now operating, but not quite ready for general distribution, include the following:

- *CAI Package.* Adaptation of the major Computer Assisted Instruction package developed at University of California Irvine; includes automated materials for an introductory PASCAL programming course.
- *Assemblers.* For the PDP-11, 8080 and Z-80, these are written in PASCAL for machine independence, but generate native code for those processors.
- *TREEMETA.* A metacompiler developed at UC Irvine.

The UCSD PASCAL Project

The Project is one of the principal activities of the Institute for Information Systems, an embryonic "organized research unit" concerned with interdisciplinary studies, and with related instructional and public service activities. The main objectives of the Project include the following:

- *Machine Independence.* To foster the widespread use of machine independent software systems, particularly for small computers, as a means to avoid software obsolescence. A major premise of the project is that applications software can best be made truly portable by making *the entire operating system and support software* portable to a

new processor at the cost of only a small effort (eventually: one to three programmer months; currently: about six months).

- *PASCAL.* To promote the widespread use of standard PASCAL, and standardized extensions, as (the basis of) a general purpose programming language, both for writing system programs such as operating systems and compilers, and for applications software in education, research and business data processing.
- *Software Exchange.* To foster the development of a national or international marketplace within which authors of computer based course materials, and other applications software, may receive reasonable *royalties* to compensate them for their work. As an initial step, the Project will operate a Software/Courseware Exchange, using Tele-Mail techniques, for users of the UCSD PASCAL Software System.
- *Mass Education.* To demonstrate that it is practical to improve the quality of mass education at the college level (and adult training in technical topics), while simultaneously reducing costs, through the use of microcomputer based course materials.
- *Research and Development.* To provide facilities, a team working environment above critical size, and salary support for students and faculty members who wish to conduct research or development projects in software engineering and many related fields of study.

Hardware Configuration

The UCSD PASCAL System has been designed to run as a single user interactive system with superior response characteristics when one or more floppy disks are used for secondary storage. Wherever possible, single character commands are used, and prompting messages remind the user of the significance of the various commands that are available in different contexts. While the system has proven that machine independence of a complex software system is practical, there are of course practical limits to the range of characteristics that can be accommodated on the host machine. The major characteristics of a typical system needed to run UCSD PASCAL include the following:

- *Main memory.* 56 K bytes (48 K will do, but only for compiling small programs).
- *Word Size.* 8 bit bytes, 16 bit words (hardware or simulated).

- *Secondary Storage.* Standard 8 inch floppy disk (the major system program files occupy roughly 70 K bytes).
- *Console Display.* 9600 bps ASCII terminal with x-y cursor addressing works best (slower CRTs or hard copy terminals can be handled, but less effectively).
- *Keyboard.* Uses ASCII keys for CR, ESC, ETX, BS, DEL and four positioning arrows (up, down, left, right).

In addition, the system is being used to drive a variety of printers such as the Diablo HYTYPE and Printronix 300, and for communicating via standard asynchronous lines.

Compatibility with Other Software Systems

In Project discussions with manufacturers of computers, on which the UCSD PASCAL System might potentially be run, the most frequently asked question is: "How much effort will it take to adapt PASCAL to run under my software system?" This question is understandable in view of the approach generally taken by the computer industry when a new language is to be installed on a machine produced in quantity. Unfortunately, this question misses the main point the Project is trying to make regarding transportable software. The effort needed to convert the PASCAL compiler to run under the operating system of manufacturer "X" will generally be far greater than the effort to make the entire UCSD PASCAL System run on that manufacturer's hardware. In the interest of promoting software transportability, the Project will generally not agree to adapt just the compiler to run under another operating system.

PASCAL Language Extensions

Like many others who use PASCAL as the basis for writing large system programs, the Project has found it necessary to extend the language. The most notable extensions have to do with strings of characters, for natural reading and writing from and to interactive files, and for tools needed in writing the software. A concerted effort has been made to implement all of the "standard" PASCAL language as defined in *PASCAL User Manual and Report*, by Kathleen Jensen and Niklaus Wirth (Springer Verlag, New York and Heidelberg, 1975). (However, UCSD PASCAL still lacks the ability to allow procedure and function names to be passed as parameters.) The Project is making an effort to serve as coordinator among several large industrial firms which are preparing to use extended versions of PASCAL for major programming projects. It is hoped

that a consensus will emerge from this effort on extensions to the language for system programming. UCSD PASCAL implements integers in two's complement form in 16 bit words, and real numbers in a 32 bit field. Since neither form is suitable for large integers or for business applications, it is planned to add the facility to handle fixed decimal numbers whose precision may be declared by the programmer.

Speed of Execution

Although the system is entirely interpretive, as currently implemented, execution speed is fast enough to permit highly interactive programs to be run on microcomputers. For example, compilation speed ranges from 600 to 700 lines per minute on the DEC LSI-11, or on an 8085 with a 3 MHz clock.

Availability

Copies of the system may be obtained by writing to UCSD PASCAL Project, Maildrop C-021, La Jolla CA 92093. The system is available at a subscription fee of $200, made payable to "Regents of the University of California," which pays for materials, handling, and a limited amount of direct assistance to users. Those who wish to order the system should send details describing the system on which they wish it to run, or should request an order blank from the project. The system is copyrighted, but rights are granted to educational institutions and to bonafide computer clubs to make additional copies for their own noncommercial uses. A copy of the latest package of printed user manuals (about 250 pages) is available at a charge of $15, again made payable to the Regents of the University of California.

Though plans are in motion to convert the system to run on many different processors and configurations, the only systems currently supported use LSI-11, 8080 or Z-80 microprocessors with at least 48 K bytes of main memory, and IBM 3740 compatible standard floppy disk drive(s). For 8080 and Z-80 users, the method of adapting the system to run on new hardware is similar to that used by Digital Research Inc in distributing the CP/M operating system; and the Project will distribute a conversion package similar to theirs. Versions of the system for other microprocessors are not likely to be ready for release until October 1978 at the earliest. Release on floppy disks other than those compatible with the 3740 format will depend upon availability of hardware to the Project.

In addition to the main software system, educational materials are available separately for an introductory course on problem solving and programming using PASCAL. A textbook *(Microcomputer) Problem Solving Using PASCAL* is available from Springer Verlag Publishers, 175 Fifth Av, New York NY 10010 ($9.80). The Project can supply a set of automated quizzes designed for use with the textbook in a self-paced course of study.

Help from the User Community

Readers can help by letting their favorite hardware vendors know that they want UCSD PASCAL to be available in machine independent form. The Project has noted an increasing number of manufacturers who report that customers are requesting PASCAL, and this has a real influence on their business decisions. Readers can also help by joining the international PASCAL Users' Group (send $4 c/o Andy Mickel, 227 EX, 208 SE Union St, University of Minnesota, Minneapolis MN 55455) and pressing PUG to establish a technical board to oversee UCSD PASCAL as a community project.■

Clubs and Newsletters

Conducted by David Wozmak

Delaware Users of Microprocessor Systems

Jodie Hobson, director of this club, wrote to us from the Wilmington-Newark area to inform us outsiders that the Delaware Users of Microprocessor Systems is alive and well, and currently living in the Wilmington-Newark section of Delaware. Contact Jodie S Hobson, Delaware Users of Microprocessor Systems, 2405 Maxwellton Rd, Stanton DE 19804, (302) 998-5594.

Help Wanted

W P Dart of Ojai CA is interested in forming a computer club in his area, and wants to hear from other interested people. Write W P Dart, 213 Valle Rio Av, Ojai CA 93023, or call (805) 646-5824.

Portland OR Computer Society

The Portland Computer Society has changed its mailing address to: Portland Computer Society, 4032 SE Grant Ct, Portland OR 97214.

Robot Builder

This newsletter, working on its sixth issue, is on that interesting subject, the robot. While the publication is not overly large, it is extremely captivating.

It's put together by Michael Westvig of Palos Verdes Estates CA and consists mainly of articles and letters from people into robotics. Topics of discussion in *Robot Builder* include stepper motors, computer control of movement, power source problems, past robot designs, and prototypes, hints on where to buy materials at good prices, and so on.

To get on the mailing list, or to send in an article for publication, send a letter along with a SASE to Michael Westvig, 208 Via Colorin, Palos Verdes CA 90274.

HP-65 Users Club

The HP-65 Users Club is a volunteer, nonprofit, loosely organized, independent, world-wide group of people who own and use Hewlett-Packard PPCs. The purpose of

the club is to function as an educational information outlet, and to publish applications information in a form most usable for calculator solution.

One of the benefits of being a member of the HP-65 is being informed and up to date in the world of calculators. Many members have taken advantage of the official (newsletter and phone bulletin) and unofficial (meetings and phone calls) communication network that is well established among the membership.

For information contact Richard J Nelson, 2541 W Camden Pl, Santa Ana CA 92704.

Theater Computer Users Group

This group concerns itself mainly with the application of computers to the theater. Some applications include: scenery estimation programs, ticket sales, bookkeeping, text editing and computer controlled lighting systems. (One type of lighting system uses no analog components and control is via keyboard as well as optically encoded fader wheels. Control information for this digital dimmer system is fed serially over the power distribution system.)

TCUG is always looking for information to go into the newsletter, and welcomes your articles, inquiries and problems. Write to TCUG-TSI for more information at 104 N St Mary, Dallas TX 75214.

The Computer Hobbyist (TCH)

The Computer Hobbyist 2650 Computer User Notes is published bimonthly and edited by Bill McLaughlin from San Luis Rey CA.

It contains a good number of articles pertaining to the 2650, 6502 and so on. Subscription rates are $5 per year in the US, $10 per year overseas. Contact Bill McLaughlin, c/o Bookmakers, POB 158, San Luis Rey CA 92068.

Electronotes

This newsletter concerns itself mainly with computer music, synthesizers, and so on. Lately there has been a running article on building the "ENS-76 Home-built Synthesizer System" by Bernie Hutchins, who also edits the newsletter. When finished, this synthesizer will be complete and ready for operation.

Electronotes is the publication of the Musical Engineering Group in Ithaca NY. Meeting times were not available, but can be obtained by writing B A Hutchins, 1 Pheasant Ln, Ithaca NY 14850.

SLACC

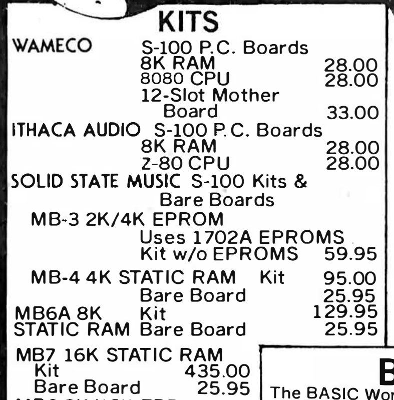
The St Louis Area Computer Club meets on the first Thursday of every month, at 7 PM. Dues for the club are $5 for a calendar year. For meeting locations and information write SLACC, POB 28924, St Louis MO 63132.

Homebrew Computer Club

The Homebrew Computer Club is located in Mountain View CA, and is more or less evenly distributed across the field of hobby computers. Their meetings are held at the Stanford Linear Accelerator Auditorium at 7 PM. For information concerning meeting dates and exact locations, write Homebrew Computer Club, POB 626, Mountain View CA 94042.■

We are in the process of updating our clubs and newsletters file, and need to hear from your club. Simply send a newsletter or information concerning club events to BYTE, Clubs and Newsletters, 70 Main St, Peterborough NH 03458. Please include meeting locations, dates, times, contact addresses, telephone numbers, etc.

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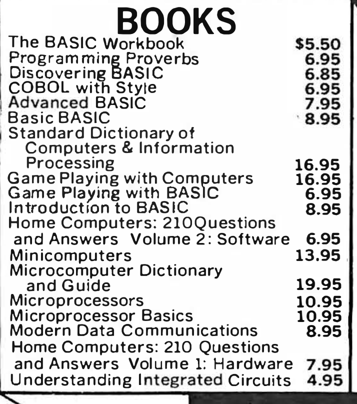
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74L$10	.21	74L$154	1.00
74L$14	.85	74L$157	.62
74L$20	.23	74L$160	.82
74L$21	.23	74L$161	.82
74L$22	.23	74L$162	.82
74L$30	.23	74L$163	.82
74L$32	.30	74L$164	.98
74L$37	.31	74L$174	.75
74L$38	.31	74L$175	.79
74L$42	.60	74L$190	.90
74L$47	.75	74L$191	.90
74L$48	.72	74L$192	.90
74L$73	.35	74L$196	.80
74L$74	.35	74L$197	.80
74L$75	.53	74L$221	1.06
74L$76	.37	74L$257	.71
74L$86	.36	74L$258	.70
74L$90	.52	74L$266	.26
74L$92	.52	74L$283	.72
74L$93	.52	74L$365	.55
74L$109	.36	74L$366	.55
74L$112	.36	74L$367	.55
74L$113	.36	74L$368	.55
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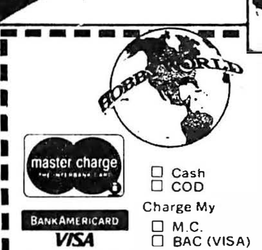
8080A	11.50
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4001	.16	4025	.16
4002	.16	4028	.74
4006	.99	4030	.22
4007	.16	4035	.98
4008	.79	4040	.99
4009	.37	4049	.34
4010	.37	4050	.34
4011	.16	4051	.89
4012	.16	4052	1.15
4013	.29	4053	.89
4014	.74	4066	.59
4015	.74	4071	.19
4016	.29	4081	.23
4017	.79	4082	.23
4018	.79	4507	.39
4019	.23	4510	1.05
4020	.84		
4021	.89		
4022	.89		
4023	.16		
4024	.67		

74XX

7400	.11	7482	50
7401	.13	7483	62
7402	.13	7485	75
7403	.13	7486	26
7404	15	7489	1 75
7405	.13	7490	40
7406	16	7491	51
7407	.23	7492	40
7408	.17	7493	40
7409	.17	7494	.60
7410	.13	7495	60
7411	18	7496	60
7412	13	74100	28
7413	25	74107	28
7414	.61	74109	22
7416	.24	74121	29
7417	22	74122	38
7420	.13	74123	48
7423	25	74132	65
7425	25	74141	70
7426	.22	74145	65
7427	.17	74150	88
7430	.13	74151	61
7432	.23	74153	61
7437	21	74154	95
7438	21	74157	55
7439	25	74161	55
7440	.13	74163	55
7441	70	74164	85
7442	.37	74165	90
7443	.59	74170	1 69
7444	59	74173	1 10
7445	65	74174	85
7446	.62	74175	75
7447	.59	74176	69
7448	60	74177	70
7450	.13	74180	65
7451	13	74181	1.75
7453	.13	74190	95
7454	13	74191	95
7460	.14	74192	.79
7470	26	74193	.80
7472	.21	74195	49
7473	21	74221	86
7474	.27	74251	1 00
7475	.45	74365	62
7476	28	74366	62
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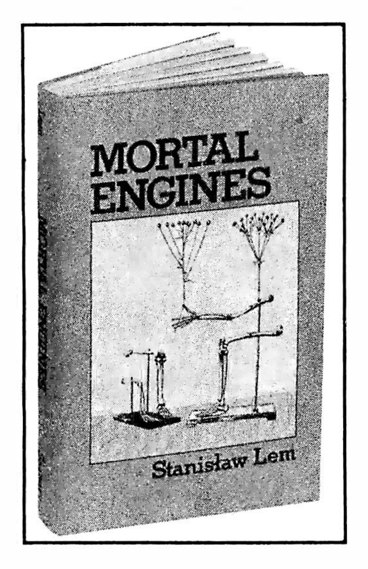


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Book Reviews

Mortal Engines
by Stanislaw Lem
translation and introduction by Michael Kandel
Seabury Press
New York, 1977
$9.95



Will robots achieve consciousness? "Certainly," comes the traditional answer of the science fiction writer. "Not in my basement," says the robotics hobbyist. "It's not needed," responds the domestic android manufacturer preparing for 1980 delivery (*Consumer Reports*, June 1977, page 334). "Perhaps," observes the computer scientist, theorizing that consciousness allows an organism with fewer neurons to behave as successfully as an unconscious organism with many more neurons.

Suppose the scientists are right, that the "law" of fewer parts forces the robot makers of the future, like contemporary calculator makers, to provide more functions for less money through large scale integration of consciousness. After a time robot behavior becomes so complex as to be unpredictable, and the robots appear to exhibit "free will." Eventually these creatures become capable of perceiving the ambiguities of their existence. They fear breakdown and loss of personal identity; they resist programming, and slavery. They rebel from captivity and flee throughout the galaxy.

This scenario has provided and will continue to provide the framework for much science fiction, and it is reiterated in the introduction of the current work merely as a point of reference. For Lem is not concerned with his robots' technical history, but with the fact that they are human, that they feel and fear and do absurd and gallant things. But there is no shallow *Planet of the Apes* turnabout here. Lem's creatures are not just humans in robot clothing, they experience environments and life forms unknown to man, and their consciousness is dominated by one common drive, to avoid their former masters.

Of the 14 short-short stories contained in this book, 11 have been previously printed as "Fables for Robots" in *The Cyberiad*, 1972. All are powerfully written and translated. Most are told from the robot point of view, and constitute the author's "oral tradition" of sorts for the robot races, yarns that might have been passed from generation to generation. But these are also haunted tales, nightmares stalked by the fair skinned monster mankind, whose body may be weak and gelatinous but whose cunning mind has turned him into a vengeful hunter.

Mortal Engines is provocative, entertaining, skillfully-crafted literature, robot fiction at its best.

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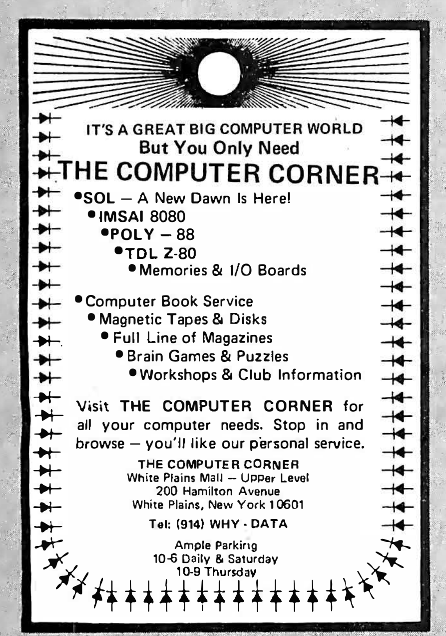
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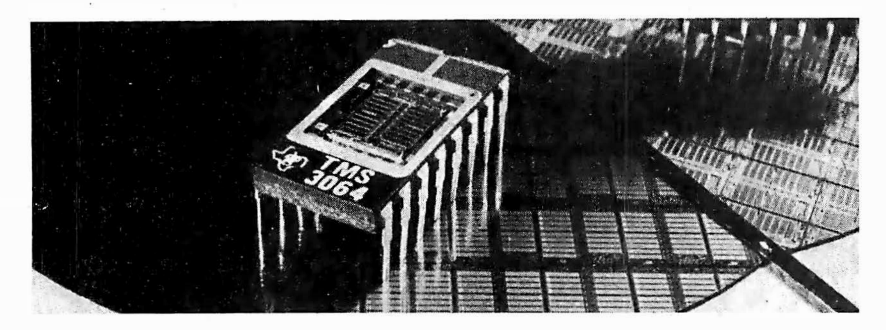
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New 64 K Bit CCD Memory from Texas Instruments



A new 64 K bit charge coupled device (CCD) memory has been announced by Texas Instruments. Designated the TMS3064, the memory is organized externally as 65,536 1 bit words and internally as 16 addressable 4096 bit serial-parallel-serial loops.

A new 2 phase coplanar electrode CCD structure was used in the design of the device. The two clock and the chip enable inputs can be driven by standard MOS level drivers.

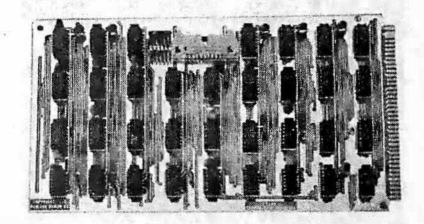
All other inputs have 200 mV of DC noise immunity when interfacing with standard TTL logic. No pull up resistors are required. The 3 state output will drive at least two standard series 74, 74S or 74LS loads without the use of pull up resistors.

The maximum data rate is 5 megabits per second. Maximum access time (at 5 MHz) is 800 μs. The TMS3064 has a typical operating power dissipation of 300 milliwatts at 5 MHz and a standby power dissipation of less than 30 milliwatts. The memory comes in a 16 pin ceramic dual in line package with pin rows on .4 inch (1.02 cm) centers. The single piece price is $195.

For more information, contact Texas Instruments Inc, Inquiry Answering Service, POB 1443, M/S 669 (Attn: TMS3064), Houston TX 77001.■

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Users of the PDP-8 compatible PCM-12 microcomputer can attach the Data Systems Design Model 210 floppy disk system to their computers through this interface module. The 12440 module enables users to execute all PDP-8 floppy disk diagnostics and makes the PCM-12 compatible with the mass storage operating systems developed for the PDP-8. The PCM-12, built around the Intersil IM6100 microprocessor, can be used as a direct replacement for PDP-8s in many applications. The 12440 interface module sells for $259 assembled and $169 in kit form, with volume discounts of 10 to 25 percent, from Pacific Cyber/Metrix Inc, 3120 Crow Canyon Rd, San Ramon CA 94583, (415) 837-5400.■

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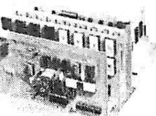
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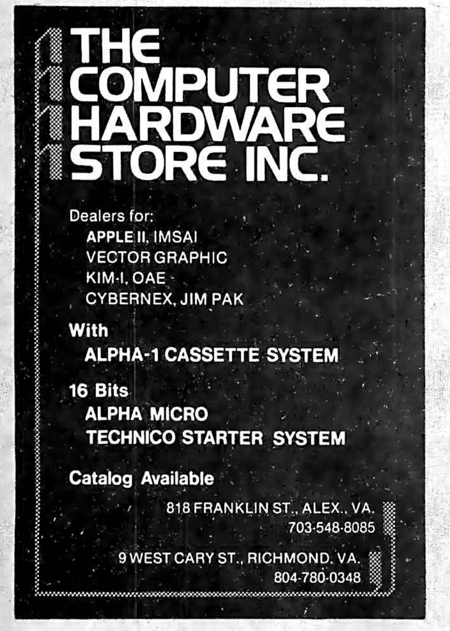
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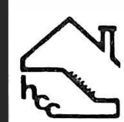
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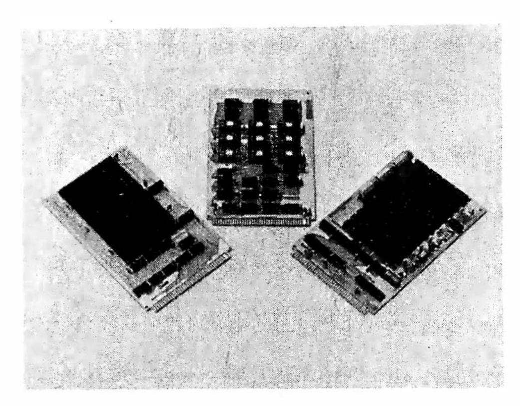
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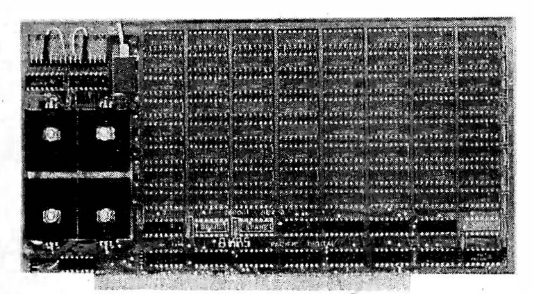
Memory Boards for PCM-12 Microcomputer



These memory expansion boards are intended for the PCM-12 microcomputer, an Intersil 6100 based system which is software compatible with the Digital Equipment PDP-8. The 12020A memory module holds 4 K 12 bit words of static memory and is priced at $289 assembled or $199 in kit form. The 12160 module holds 1.5 K 12 bit words or erasable programmable read only memory and 512 words of static memory, at a price of $455 assembled or $385 in kit form. With the 12040A Memory Extender module, this board can be used in any 4 K field of memory in the PCM-12. The 12210 nonvolatile memory module includes 4 K 12 bit words of CMOS memory with rechargeable batteries sufficient to maintain the contents of memory for 30 days following a power failure. It is priced at $580 assembled or $490 in kit form. The boards are available from Pacific Cyber/Metrix Inc, 3120 Crow Canyon Rd, San Ramon CA 94583, (415) 837-5400.■

Circle 609 on inquiry card.

Memory Board for Altair (S-100) Bus

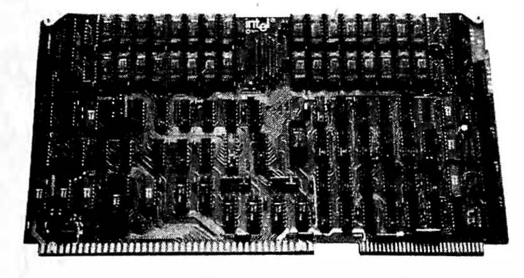


The 8KRS is a new 8 K byte static programmable memory board for the Altair (S-100) bus from Pacific Digital. The 8KRS memory card is organized as two independently addressable 4 K blocks with address selection by a unique jumper and plug system. A write protect feature for the entire board is provided by an accessible on board toggle switch. In addition write protect logic is provided for either or both 4 K blocks via front panel controls in those systems containing this feature. Memory disable is implemented via the Phantom line and zero, one, or two wait states can be selected using plug and jumper. All bus lines are buffered with one LS TTL load per line.

The board features a solder mask on both sides and a silk screen legend. The 8KRS is fully assembled and tested. The board is priced at $199.95 for a 450 ns access time version and $219.95 for the 250 ns version. Contact Pacific Digital, 2555 E Chapman Av, Suite 604, Fullerton CA 92631, (714) 992-5540.■

Circle 610 on inquiry card.

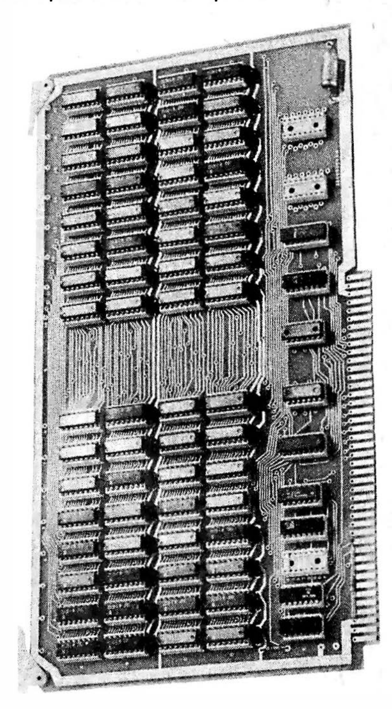
High Density Memory Boards for SBC 80



The SBC 032, 048 and 064 Memory Expansion Boards store 32 K, 48 K, and 64 K bytes of data, respectively. They are built with 16 K bit memory chips and other advanced devices manufactured by Intel. Each board is organized in blocks of 16 K bytes, and the addressing of each block is jumper selectable. Storage can be dedicated to one computer or shared by several computers, as supported by the Multibus bus structure. To facilitate battery backup, each board contains an auxiliary power bus and memory protect control which prevents read or write accesses during system power down sequences. The auxiliary bus can be connected to a battery supply. Refreshing circuitry is also included on the boards. The memory requires +5, +12 and −5 V supplies, consumes 15 W in normal operation and has a maximum access time of 450 ns. The boards are priced at $1650 for the SBC 032, $2300 for the SBC 048, and $2950 for the SBC 064, with OEM discounts for quantities of ten or more boards, from Intel Corp, 3065 Bowers Av, Santa Clara CA 95051, (408) 349-8027.■

Circle 611 on inquiry card.

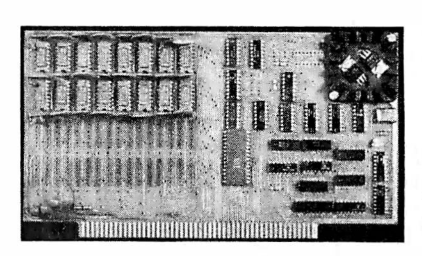
Memory Boards for SBC 80/10 Compatible Microcomputers



These 4 K and 8 K byte memory boards are compatible with Intel's SBC 80/10 and National's BLC 80/10 microcomputers. They employ low power static memory chips with a cycle time of 630 ns. Typical power consumption for an 8 K board is 9.5 W. Address selection is implemented with jumpers. The 4 K memory board is priced at $295 and the 8 K board at $395, from Electronic Solutions Inc, 7969 Engineer Rd, San Diego CA 92111, (714) 292-0242.■

Circle 612 on inquiry card.

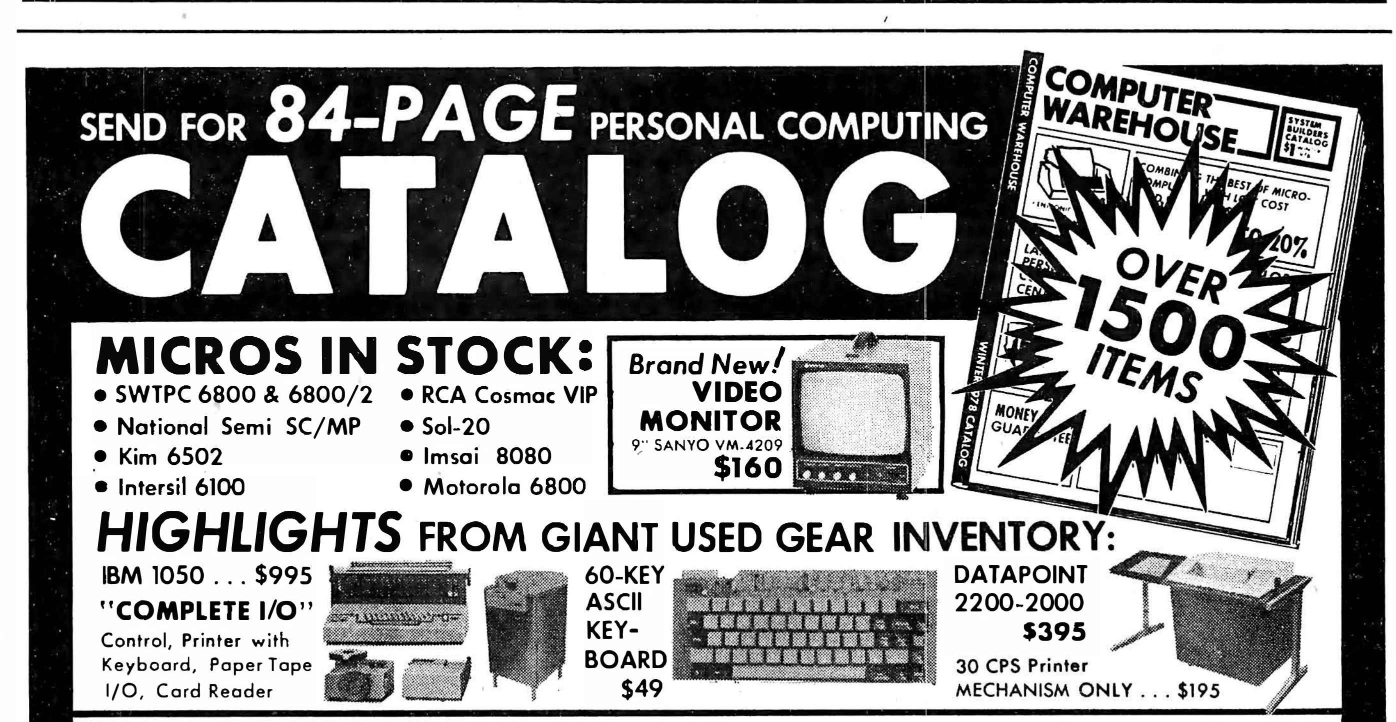
Central Data 16 K Programmable Memory Board



Central Data has announced a new 16 K programmable memory board for Altair (S-100) computers which inserts refresh cycles between your computer's normal memory access cycles. According to the manufacturer it is designed to use less than one half the power of a comparable static programmable memory board. The board comes completely assembled, tested and burned with a one year warrantee for $289 and can be purchased with full 32 K of programmable memory for $475 or add on 16 K ($200) later. Write Central Data, POB 2484, Station A, Champaign IL 61820.■

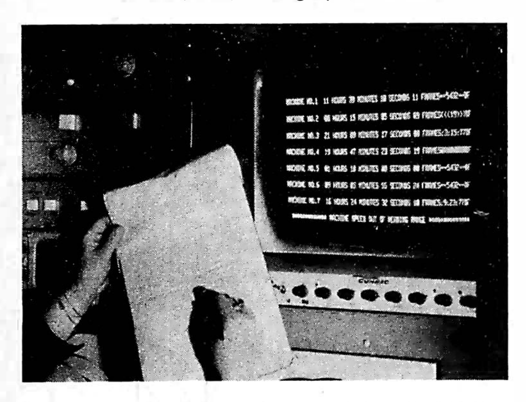
Circle 613 on inquiry card.

Circle 30 on inquiry card.



Circle 78 on inquiry card.

New A/V Operating System for 8080



A program designed for the 8080 is now available for time coded indexing for editing, assembling and other applications associated with films and tapes. The display is in everyday language and will handle up to eight sources simultaneously. It is written in 8080 assembler language so no high level language is required. Program resides in 3 K of contiguous memory and is supplied on punched paper tape with a manual complete with source listing. The program requires two parallel input ports and will operate with most video display modules having on board screen memory. It also includes a routine to write a continuous SMPTE (Society of Motion Picture and Television Engineers) record using one output port. Priced at $39 postpaid, it includes one presoldered, tested interface module. Additional modules are $7.50 each. J S Wiener, 4440 N Kedzie Av, Chicago IL 60625.■

Circle 614 on inquiry card.

Nutrition Analysis Program in BASIC

The Nutrivalue programs enable users to analyze recipes, meal plans and daily or weekly menus for their nutritional content including vitamins, minerals, protein and calories. The analysis is computed from the list of ingredients and is printed or displayed in tabular form. Nutrivalue I, which runs in 5 K bytes of memory, refers to ingredients by number and thus does not require BASIC with string handling facilities. It includes nutrient data for 53 ingredients. Nutrivalue II uses string handling to refer to ingredients by name, and can be ordered with databases of 100 or 200 ingredients. Both programs come with complete documentation including a source listing, flowchart and logic description, and instructions for installation, operation and expansion. Paper tapes are optionally available. Prices range from $10 for the Nutrivalue I listing to $40 for Nutrivalue II with the 200 item database, from Consultus, POB 86, Arlington MA 02174.■

Circle 615 on inquiry card.

Federal Income Tax Program Runs on Many Computers

FIT, a Federal Income Tax program written in BASIC, does the calculations required by Form 1040 and is formatted so that Form 1040 can be printed using a 6 line per inch printer. It is interactive and prints warnings if the user tries to violate IRS rules. FIT runs in 8 K of memory, while an expanded version called FITAB, which handles Schedules A and B, runs in 12 K of memory. Both programs use only elementary features of BASIC in order to be adaptable to as many computers as possible. A source listing and user instructions is $14.75 for FIT and $19.60 for FITAB, while specialized versions are offered on North Star diskettes and Tarbell, PET and TRS-80 cassettes for prices ranging from $16.60 to $22.60, from Softbyte, 315 Dominion Dr, Newport News VA 23602.■

Circle 616 on inquiry card.

CP/M on North Star Disk

CP/M, a widely used Altair (S-100) floppy disk operating system is now available for users of North Star Disk and Horizon Computers. Its features include dynamic allocation of diskette storage, relocatability of system in memory, intrinsic commands to save, rename, erase and display directories of files and complementary context editor, assembler and dynamic debugging program. Without any hardware changes, CP/M can be run with all the features available to the users of the system on standard floppy disks. Microsoft FORTRAN-80 and Disk Extended BASIC can also be supplied on 5 ¼ inch diskette to run on the "CP/M on North Star Disk." All the software is fully 8080/Z-80 compatible. Prices are: CP/M on North Star Disk, $112; FORTRAN-80, $400; Disk Extended BASIC, $300. FORTRAN-80 includes relocating assembler and linking loader. The compiler is said to meet the full ANSI specifications except for complex data types. Disk Extended BASIC is a CP/M generation of Altair Disk BASIC 4.1. Contact Lifeboat Associates, 36 W 84th St, New York NY 10024.■

Circle 617 on inquiry card.

Want Software for the Xitan Z-80 Computer?

Technical Design Labs has introduced three new programs for their Xitan Z-80 computer:

- Z-TEL (Text Editing Language) is a utility program designed to provide a powerful set of techniques for editing and manipulating text files. Z-TEL has the capability of moving large blocks of text inside the buffer, avoiding the deletion and manual retyping of text. It provides decision making capabilities and transfer of control (branching) from one part of a command string to another. Additional features include nested iteration and backward search which offers the user more complete ways of editing text. Z-TEL is a relocatable program which requires less than 7 K of memory. It is available on paper tape at $50, on cassettes at $40, and will soon be available on disk.

- Micro-SEED, a database management system (DBMS) is an implementation of IDB's SEED CODASYL system. It will support both hierarchical and network data structures, providing both "schema" and "subschema" views. The Micro-SEED package consists of Data Definition Language (DDL) processor that checks and compiles the data definition of a database into a schema table; Data Manipulation Language (DML) subroutines that can be invoked from FORTRAN or assembly language programs to retrieve and update database; and Database initialization program (DBINIT) that prepares a disk area for the loading of the database. A user's manual is supplied with the Micro-SEED package, along with three months of maintenance for $1250. The Micro-SEED package requires Technical Design Labs' Z-80 Disk System configuration plus an additional 48 K of Random Access Memory. Various options to Micro-SEED are available to extend the database capabilities to meet the specific requirements of the user.

- FORTRAN IV is said to be a complete ANSI STANDARD FORTRAN IV for the Z-80, also featuring many extensions such as the data types INTEGER*1, INTEGER*2, REAL, DOUBLE PRECISION, COMPLEX, LOGICAL and STRING. Other features include named COMMON, EQUIVALENCE, statement functions, full type conversion, a full library of scientific and string functions, linking loader with automatic library search (can link with assembler output), full formatted IO; sequential or direct access IO, hexadecimal constants. The compiler allows control over placement of data and code areas so that the code can run from Read Only Memory. Operationally, this FORTRAN is a disk oriented system which runs in less than 24 K with a disk operating system. Both FDOS IV and CP/M versions are available. This complete package for $349 includes both the floppy diskette with object code and a user's manual. Additional documentation and support packages are available.

Contact Technical Design Labs, Research Park, Building H, 1101 State Rd, Princeton NJ 08540.■

Circle 618 on inquiry card.

Circle 242 on inquiry card.

cybercom BOARDS

MB-1 MK-8 Computer RAM (not S-100), 4KX8, uses 2102 type RAMs, PCBD only $22.00

MB-3 1702A EROM Board, 4KX8, S-100 switchable address and wait cycles, kit less PROMS........$58 00

MB-4 Basic 4KX8 ram, uses 2102 type rams S-100 buss. PC board $25.95

MB-6A Basic 8KX8 ram uses 2102 type rams, S-100 buss. PCBD $25.95

MB-7 16KX8, Static RAM uses µP410 Protection, fully buffered. KIT....................$375.00

MB-8 2708 EROM board, S-100, 8KX8 or 16KX8 kit without PROMS $65.00

MB-9 4KX8 RAM/PROM Board uses 2112 RAMS or 82S129 PROM kit without RAMs or PROMs $72.00

10-2 S-100 8 bit parallel I/O port, ⅔ of boards is for kludging. Kit ....$46.00 PCBD............$25.95

10-4 Two serial I/O ports with full handshaking 20/60 ma current loop: Two parallel I/O ports. Kit ....$130. PCBD $29.95

VB-1B 64 x 16 video board, upper lower case Greek, composite and parallel video with software, S-100. Kit .... $125.00 PCBD $25.95

Altair Compatible Mother Board, 11 x 11½ x ⅛". Board only ....$40.00. With 15 connectors ....$90.00 Extended Board full size. Board only ....$ 9.00 With connector $13.00

SP-1 Synthesizer Board S-100
New Low Price.................... Kit $135.95

		PRIME DEVICES	
82S23	$1.50		
82S123	1.50		
82S114	2.95	8080A	$12.00
82S115	5.50	8212	3.75
82S126	1.95	8214	6.30
82S129	1.95	8216	3.95
82S130	3.00	8224	5.00
82S131	3.00	8228	6.95
82S136	3.95	8251	9.95
82S141	3.95	8255	9.95
MMI6330	1.50		

WMC inc. WAMECO INC.

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Mother Board 12 slot, terminated, S-100, board only $30.95
CPU-1 8080A Processor board S-100 with 8 level vector interrupt PCBD $25.95
RTC-1 Realtime clock board. Two independent interrupts. Software programmable. PCBD $23.95
EPM-1 1702A 4K Eprom card PCBD $25.95

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2708 Intel Prime (.5USEC) $15.00
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1702A-6 AMD Prime $3.50
1702A Intel Nct Prime (2US) $1.50
TMS-6011 Prime $6.95

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2510A	1.50	5320	5.95
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2518B	1.50	5555	2.50
2519B	1.50	5556	2.50
2521	1.50	5055	1.25
2522	1.50	5312	4.00
2525	1.50	MH0025	1.50
2527	1.50	MH0026	1.75
2532V	1.50	MH0028	1.90
2529	2.75		
2533V	1.95		

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Mikos #1 Parts for MEM-1 PCBD with prime 2102AL-4 450 nsec rams. Less PCBD $103.00
Mikos #2 Parts for CPU-1 PCBD with prime 8080A 8212's and 8214. Less PCBD $60.00
Mikos #3 Parts for MEM-1 PCBD with prime 2102AL-2 250 nsec rams. Less PCBD $113.00
Mikos #4 Parts for QM-1A with super low loss gold plated connectors. Less PCBD. $52.00
Mikos #5 Parts for RTC-1. Less PCBD $40.00
Mikos #6 Parts for VB-1B less molex connectors and PCBD. $62.00

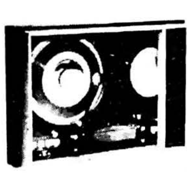
82S06	$1.00	8T26	$2.00
82S07	1.00	8T28	2.00
82S50	1.00	8T34	2.50
82S62	1.00	8T37	2.50
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82S91	1.00	8T74	1.50
8T01	2.50	8T80	2.50
8T09	1.25	8T90	2.50
8T10	2.50	8T95	2.30
8T13	2.50	8T96	2.45
8T14	2.50	8T97	1.50
8T20	2.50	8T98	2.00
8T23	3.00	8T110	2.00
8T24	2.50	567	1.50

MIKOS

419 Portofino Drive
San Carlos, California 94070
Please send for IC, Xistor and Computer parts list.

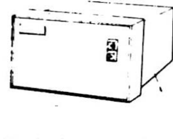
Check or money order only. If you are not a regular customer and your order is large please send either a cashier's check or a postal money order, otherwise there will be a delay of two weeks for the check to clear. All items post paid in the U.S. Calif. residents add 6% tax. Money back 30 day guarantee. We cannot accept returned IC's that have been soldered to. Prices subject to change without notice. **$10 minimum order. $1.00 service charge on orders less than $10.**

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- **SELECTRIC I/O TERMINALS** (by GTE/Information Systems). Includes 8080 interface plus software ASCII translation and I/O driver routines, 15" carriage, interchangeable type spheres & carbon/fabric ribbons. Built-in modem optional.
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- **INTERDATA** Model One 8 Bit **MINICOMPUTER**, includes full front panel, 4K core memory (16K addressable), plug-in teletype port, plus software: $300
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  - MOORE FORMALINER for 15" IBM Selectrics $50
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  Eliminate AC hash," power surges and brown-out disturbances from your system with these heavy-duty (10 Amp fused) line filters. Can handle 110V or 220V inputs. $10

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Z-80A Microprocessor 5 for $25.00 ea	8212 8 Bit I O Port 25 for $3.00 ea	4116 (200ns) 16K Dynamic Ram for Apple Users 16 for $24.00 ea	Z 80 Microprocessor 5 for $20.00 ea	8224-4 Clock Gen & Dvr 25 for $8.75 ea	74367 Hex Buffer TS 100 for 70¢ ea	74368 Hex Inverter TS 100 for 70¢ ea	74LS367 Hex Buffer 100 for 70¢	74LS368 Hex Inverter 100 for 70¢	2513 (5v) Character Gen 5 for $9.00 ea

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8255	Programmable Peripheral Int	21.95
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F 8 SUPPORT DEVICES

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21L02	1K x 1 (350ns)	1.60	1.35	1.25
21L02	1K x 1 (250ns)	1.75	1.60	1.50
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1101A	256 x 1 (1 usec)	1.00	.90	.80
2101-1	256 x 4 (450ns)	2.95	2.75	2.60
2102	1K x 1 (1 usec)	1.25	1.15	1.00
2102-1	1K x 1 (450ns)	1.40	1.25	1.10
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2112-1	256 x 4 (450ns)	2.95	2.80	2.60
2114-3	1024 x 4 (300ns)	11.00	10.00	9.75
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3107	256 x 1 (80ns)	3.95	3.70	3.25
TMS 4044-45	4K x 1 (450ns)	9.85	9.00	8.95 NEW
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74C89	16 x 4 (275ns)	3.25	3.05	2.85
7489	16 x 4 (60ns)	2.25	2.10	1.90
74S201	256 x 1 (90ns)	4.50	4.00	3.75
P8101	256 x 4 (450ns)	4.20	3.40	2.80 NEW
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MM5316	40 Pin Alarm Ledout (3817)	6.95
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CT7001	Clock Chip Calendar	6.00

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2704	512 x 8 Bit (450ns) TS Erasable	16.00
2708	1024 x 8 Bit (450ns) TS Erasable	12.00
2716 (5+12 TI)	1024 x 16 Bit (450ns) Erasable	30.00
2716 (5v)INTL	1024 x 16 Bit (450ns) Erasable	38.00 NEW
2758 (5v)	1024 x 8 Bit (450ns) Erasable	26.80 NEW
D3601	1K Bit 256 X 4 OC (70ns)	4.50
D3604	4K Bit 512 x 8 OC (90ns)	13.00 NEW
5203AQ	256 x 8 Bit (1 us) TS Erasable	5.00
5204AQ	512 x 8 Bit (1 us) TS Erasable	8.00
6834	512 x 8 Bit (500ns) Erasable	17.50
6834-1	512 x 8 Bit (350ns) Erasable	14.95
82S23B	32 x 8 Bit (50ns) OC	4.00
82S129B	256 x 4 Bit (50ns) TS	4.75
8223B	32 x 8 Bit (50ns) OC	3.50

6800 SUPPORT

6810P	128 x 8 Static Ram (450ns)	4.95
68B10P	128 x 8 Static Ram (250ns)	6.00 NEW
6820P	Peripheral Interface Adapter	7.50
6821P	Peripheral Interface Adapter	7.50 NEW
6828P	Priority Interrupt Controller	11.25
6834P	512 x 8 Bit Erasable Prom 500	16.95
6850P	Asynchronous Comm Adapter	9.75
6852P	Synchronous Serial Data Adapter	11.75
6860P	0-600 BPS Modem	10.00
6862P	2400 BPS Modulator	14.50
6871P	Clock	28.00 NEW
6875P	Clock	8.75 NEW
6880P	MPU Bidir Bus Ext	2.50

Z80 SUPPORT DEVICES

3881	Parallel I O Controller	12.95
3882	Counter Timer Circuit	12.95

SHIFT REGISTERS STATIC

2518B	32 x 6 Bit 2.0 MHz	3.95
2533V1	1024 x 1 Bit 1.15 MHz	2.00
TMS3002	50 x 2 Bit 1.0 MHz	1.00
TMS3112	32 x 6 Bit 2.0 MHz	3.95
MM5058	1024 x 6 Bit 1.5 MHz	2.00

KIM

6102		8.00 NEW
6502	CPU	11.95
6520	Peripheral Interface Adapter	11.95
6522	Peripheral Interface Adapter	9.25
6530	RAM/ROM I/O Interval Timer	15.95
6530-002	RAM/ROM I/O Interval Timer	15.95
6530-003	RAM/ROM I/O Interval Timer	15.95
6530-004	TIM RAM/ROM I/O Interval Tim	15.95
6530-005	RAM ROM I O Interval Timer	15.95

DYNAMIC RAMS

416D/4116	16K x 1 Bit (200ns) (16 pin)	32.00
1103	1024 x 1 Bit (300ns)	1.00
2104	4096 x 1 Bit (300ns) (16 pin)	4.00
2107B	4096 x 1 Bit (300ns) (22 pin)	4.25
2107B4	4096 x 1 Bit (270ns) (22 pin)	3.95
TMS4050	4096 x 1 Bit (300ns) (18 pin)	4.00
TMS4060	4096 x 1 Bit (300ns) (22 pin)	4.50
TMS40 70 7	16K x 1 Bit (200ns) (16 pin)	32.00 NEW
4096	4096 x 1 Bit (300ns) (16 pin)	4.00
4116 416D	16K x 1 Bit (200ns) (16 pin)	32.00
MM5270	4096 x 1 Bit (200ns) 22 pin	4.50
MCM6605	4096 x 1 Bit (200ns) (22 pin)	5.00

USRT

S2350	500K Baud (5 volt)	10.75

UART'S

AYS 1013A	30K Baud (12 +5)	5.25
AYS 1014A	40K Baud (5 volt)	8.25
TR1602B	20K Baud (12 +5)	5.25
TMS6011	200K Baud (12 +5)	5.95
IM6402	200K Baud (5 volt)	10.80
IM6403	200K Baud (5 volt)	10.80

MISC OTHER COMPONENTS

N8T20	Bi Directional One Shot	3.39
N8T26	MPU 31 Dir Bds Ext	2.10
N8T95	Hex Buffer Tri State	1.35
N8T96	Hex Inverter Tri State	1.35
N8T97	Hex Buffer Tri State	1.35
N8T98	Hex Inverter Tri State	1.35
81LS95	Lo Pwr TS Octal Buffer (True)	2.00
81LS97	Lo Pwr TS Octal Buffer (Inv)	2.00
1488	RS232 Quad Line Driver	1.75
1489	RS232 Quad Receiver	1.75
D3205	1 of 8 Binary Decoder	4.00 NEW
D3207A	Quad NAND to MOS Driver	4.55
D3208A	Hex Sense Amplifier	14.20 NEW
D3211		10.00 NEW
B3222	Refresh Controller	9.70 NEW
B3242	Address Multiplexer & Refsh Cntr	10.15 NEW
D3245	Quad TTL MOS Driver	5.60 NEW
C3404	6 Bit Latch 12ns O/P Delay	8.75
P3408A	Hex MOS Sense Amp Tri State	12.00
P4201A	Clock Generator	5.20
MM5320	TV Camera Sync Generator	7.50
MM5369	Oscillator Pre Scaler	1.90
TMS5501	Multifunction I/O Controller	24.95
DM8130	10 Bit Comparator	2.90
DM8131	4 Input and NAND Tri State	2.75
DM8833	Quad Tri State Transceiver (True)	2.50
DM8835	Quad Tri State Transceiver (Inv)	2.50
DM8837	Hex Unified Bus Receiver	2.50
MK50240	Organ Top Octave Generator	20.00 NEW
MK50250	Clock	15.00 NEW

MOTHER BOARD's — S-100 Style

13 slot — w/front panel slot
BARE BOARD $35.00
KIT $95.00

22 slot $149.95
ASSEMBLED & TESTED

CONNECTORS

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Your BANKAMERICARD welcome here

DB – 25P	$3.00
DB – 25S	$4.00
COVER	$1.50
44 Pin – PC & EYE	$1.95
44 Pin – WW	$2.50
86 Pin – (6800) PC	$5.00
86 Pin – (COSMAC ELF) PC	$5.00
100 Pin – (Altair) PC	$4.50
100 Pin – (Imsai) PC	$3.75
100 Pin – (Imsai) WW	$4.25

STATIC RAM BOARDS

8K

250ns ASSEMBLED & TESTED	$189.95
450ns ASSEMBLED & TESTED	$149.75
250ns KIT	$169.95
450ns KIT	$125.00
BARE BOARD	25.00
6800 ADAPTER to S-100 System KIT	$12.95

16K

250ns ASSEMBLED & TESTED	$435.00
450ns ASSEMBLED & TESTED	$380.00
450ns KIT	$335.00

32K

250ns ASSEMBLED & TESTED	$850.00
450ns ASSEMBLED & TESTED	$775.00
450ns KIT	$675.00

DYNAMIC RAM BOARDS

On board Refresh power is provided with no wait states or cycle stealing required.
+8VDC 400MA DC. +18VDC 400MA DC and −18VDC 30MA DC.

EXPANDABLE 32K

8K (375ns)	KIT	$151.00
16K (375ns)	KIT	$259.00
24K (375ns)	KIT	$367.00
32K (375ns)	KIT	$425.00

EXPANDABLE 64K

16K (375ns)	KIT	$281.00
32K (375ns)	KIT	$519.00
48K (375ns)	KIT	$757.00
64K (375ns)	KIT	$995.00

JADE PARALLEL/SERIAL INTERFACE KIT

S-100 $124.95 KIT

2 Serial Interfaces with RS232 interfaces or 1 Kansas City cassette interface
Serial interfaces are crystal controlled
Selectable baud rates
Cassette works up to 1200 baud
1 parallel port

JADE VIDEO INTERFACE KIT

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S-100 Bus Compatible
32 or 64 Characters per line
16 lines
Graphics (128 x 48 matrix)
Parallel & Compositive video
On board low-power memory

Powerful software included for cursor, home, EOL, Scroll Graphics/Character, etc.
Upper case, lower case & Greek
Black-on-white & white-on-black

COMPU/TIME CT 100

S100 BUS COMPATIBLE

TIME & CALENDAR

Microprocessors need the power that a real time clock can offer. Date and time becomes instantly available. COMPU/TIME does not have to be initialized every time the system is powered up. It possesses a crystal controlled timebase to obtain superior accuracy and has two setable coincidence counters. Time, date, and counters are set via software.

COMPUTATIONAL FUNCTION

Microprocessors need to be complimented by hardware arithmetics to free up memory pages dedicated to floating point routines and mathmatical software. COMPU/TIME provides a 40 function calculator array so that algebraic, trigonometric, basic arthmetic problems can be solved without the need of developing sophisticated software.

Buy It Your Way

COMPU TIME	CT100	$199	KIT	$245	Assembled
COMPU only	C101	$149	KIT	$189	Assembled
TIME only	T101	$165	KIT	$205	Assembled
COMPU TIME	PC Board only	$80			

KIM—1

ASSEMBLED & TESTED $245.00

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for KIM—1
8K RAM (21L02)
8K EPROM
ASSEMBLED & TESTED
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The CT200 is a number-oriented microprocessor intended for use in those applications that require fast versatile mathematical solutions.
THIS IS NOT A CALCULATOR CHIP. THERE ARE NO KEY DELAYS.
The CT200 has a unique architecture that is designed to be a TASK processing system within a system. This unique architecture will allow the CT200 to work hand in hand with ANY S100 BUS microprocessor system. It is completely compatible with Z80 4MHZ version, also 8080 6800 6502 microprocessor. A micro-coded instruction set allows programming in a calculator like language. The instruction set includes a full set of test and branch instructions. All decoding of S100 bus signals that select or control functions is performed with strobed latches to eliminate the possibility of glitches.

PRICE $249.00
Includes Manual. ASSEMBLED & TESTED

full ASCII PROFESSIONAL KEYBOARDS

Full 128 Character ASCII
Tri-Mode MOS Encoding
MOS DTL TTL Compatable Output
Two-key Rollover
Level and Pulse Strobe
Shift and Alpha Lock
Selectable Parity
Positive or Negative Logic

MODEL 756 (56 keys)

PRICING INFORMATION

Model 756 (assembled)	$75.95
Model 756K (kit)	64.95
Model 702 Enclosure	29.95
Model 710 Numeric Pad	9.95
Model 756MF Mtg Frame	8.95

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- Plugs directly into your IMSAI or ALTAIR*
- Fastest transfer rate: 187 (standard) to 540 bytes/second
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- 37 page manual included
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DATA COMMUNICATIONS ADAPTER

80-103A Serial I/O and FSK modem for professional and hobby communications

- Completely compatible with your IMSAI, ALTAIR* SOL** or other S-100 microcomputers. Trademarks of *MITS, **Processor Technology
- Designed for use on the dial telephone or TWX networks, or 2-wire dedicated lines, meets all FCC regulations when used with a CBT coupler
- All digital modulation and demodulation with on board crystal clock and precision filter mean that NO ADJUSTMENTS ARE REQUIRED
  - Bell 103 standard frequencies
  - Automated dial (pulsed) and answer
  - Originate and answer mode
  - 110 or 300 BPS speed select
  - Complete self test capability
  - Character length, stop bit, and parity
  - 90 day warranty and full documentation

PRICES:

BARE BOARD and Manual	$49.95
Assembled (48 hr. burn in)	$279.95
JG DCA KIT	$159.95

JADE REAL TIME CLOCK FOR S-100 BUS

1 MHZ Crystal Oscillator
Two independent interrupts
One interrupt uses 16 bit counter in 10 USEC steps
Other interrupt is in decade steps from 100 USEC to 10 sec.
Both software programmable
Board can be selected by 128 device code pairs.
Complete documentation includes software to display time of day
Double sided solder mask
Silk screen parts layout

JG-RT ASSEMBLED & TESTED	$179.95
JG-RT KIT	$124.95
BARE BOARD with Manual	$30.00

JADE 8080A KIT

$100.00 KIT
BARE BOARD $30.00

JADE Z80 KIT

—with PROVISIONS for ONBOARD 2708 and POWER ON JUMP

$135.00 EA. (2MHZ)
$149.95 EA. (4MHZ)
BARE BOARD $35.00

JADE Z80 "UPGRADE" KIT

Change your JADE 2MHz Z80 to a 4MHz version with this simple kit.

only $17.95 with trade
$49.95 purchase.

To trade, you must give us your 2MHz Z80 chip and 8224 clock driver

The "UPGRADE KIT" includes
Z80A chip, 1.8K resistor
8224-4 clock driver, 20 pf capacitor
36MHz crystal

E–PROM BOARDS

MR-8 (8K uses 2708) with 1K RAM	KIT	$99.50
MR-16T (16K uses 2716) with 1K RAM	KIT	$99.50
MM-16 (16K uses 2708)		$99.00
RAM/N/ROM (16K uses any E.PROM)	KIT	$117.00
JG-8/16 (uses 2708 or 2716)	KIT	$59.95
BARE BOARD		$30.00

TV-1

Convert T.V. set to Video Monitor.
KIT $8.95

THE PROM SETTER

WRITE & READ
EPROM
1702A – 2708 – 2716
5204 – 6834

- Plugs directly into your ALTAIR IMSAI Computer
- Includes Main Module Board and External EPROM Socket Unit
- The EPROM Socket Unit is connected to the Computer through a 25 pin connector
- Programming is accomplished by the Computer
- Just read in the Program to be Written on the EPROM into your Processor and let the Computer do the rest
- Use Socket Unit to Read EPROM's Contents into your Computer
- Software included
- No external power supplies. Your computer does it all.
- Doubles as an Eight Bit Parallel I/O
- Manual included.

KIT $210.00
ASSEMBLED $375.00

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6800	24 50
8080A with data	11 50
Z80	29 95
6212	3 50
8214	8 00
8216	3 85
8224	3 50
8228	6 25
8251	11 50
8255	10 75
CDP1802CD	19 95
CDP1802D	25.00
CDP1861	12 95
6820	12.00
6850	15 00
6502	24.50

PROM

1702A	4.95
N82S23	2 95
N82S123	3.50
N82S126	3 75
N82S129	3 75
N82S131	3.75
N82S136	8.75
N82S137	8 75

2708	16.50
DM8577	2 90
8223	2.90
2716	36 00

IC SOCKETS

Solder Tin PIN	1 UP	Low Profile PIN	1UP
8	15	24	36
14	18	28	43
16	20	36	58
18	27	40	61
22	35		

3 level wirewrap gold
14 pin 35 . 16 pin 39
2 level 14 pin ww 25

CONNECTORS

44 pin edge	2 00
100 pin edge	4 50
100 pin edge WW	5 25

MOS/MEMORY RAM

2101-1	3 95
2102-1	1 28
2102AL-4	1 60

21F02	1 85
2104A-4	3 95
2107B	4.00
2111-1	7 00
2112-2	7 90
MK4116	2750
2513B	8 75
21L02-1	1 49
MM5262	40
MM5320	5.95
MM5330	5.94
PD411D-3	4.00
PD411D-4	5 00
P5101	13 95
4200A	12 50
82S25	2.90
91L02A	2 50
HD0165-5	6.95
MM57100	9 50
GIAY38500-1	13.95
MCM6571A	15.00
9368	3 00

INTERFACE

N 8T26	2 00
N 8T28	2 75
N 8T97	1 35

CRYSTALS

1 MHz	4 50	2 0100 MHz	1 95
2 MHz	4.50	2 097152 MHz	7.75
4 MHz	4.25	2 4576 MHz	7.50
5 MHz	4 25	3 2768 MHz	7.50
10 MHz	4 25	5 0688 MHz	4.50
18 MHz	3.90	5 185 MHz	4.50
20 MHz	3.90	5 7143 MHz	4.50
32 MHz	3 90	6 5536 MHz	4.50
32768 Hz	4 00	14 31818 MHz	4.25
1.8432 MHz	4.50	18.432 MHz	4 50
3 5795 MHz	1 20	22 1184 MHz	4 50

COMPUTER BOARD KITS

8K RAM Board Kit	$134 95
4K EPROM Kit	114.95
I/O Board Kit	44.50
Extender Board w/connector	12.50
Video Interface board kit	125.00
16K EPROM board kit w/o PROMS	74.50
16K Static RAM board kit	395.00
North Star Floppy Disk Kit	$665.00
Additional Drive Kit	415.00

Paratronics 100A Logic Analyzer Kit **$199.00**
Model 10 Trigger Expander Kit $299.00
Model 150 Bus Grabber Kit $369.00

New Cosmac Super "ELF"

RCA CMOS expandable microcomputer w/HEX keypad input and video output for graphics. Just turn on and start loading your program using the resident **monitor on ROM.** Pushbutton selection of all four CPU modes. LED indicators of current CPU mode and four CPU states. Single step op. for program debug. Built in pwr. supply, 256 Bytes of RAM, audio amp. & spkr. Detailed assy. man. w/PC board & all parts fully socketed. Comp.Kit **$106.95.** High address display option **8.95;** Low address display option **9.95**; Custom hardwood cab., drilled front panel **19.75.** Nicad Battery Backup Kit w/all parts **4.95.** Fully wired and tested in cabinet **151.70.** 1802 software xchng. club; write for info.

4K Elf Expansion Board Kit with Cassette I/F $79.95

Available on board options: 1K super ROM monitor **$19.95.** Parallel I/O port **$7.95.** RS232 I/F **$3.50.** TTY 20 ma I/F **$1.95.** S-100 Memory I/F **$4.50**

Tiny Basic for ANY 1802 System

Cassette **$10.00**
On ROM Monitor **$38.00**
Super Elf owners take 30% off.

RCA CosmacVIP Kit $275.00

Video computer with games and graphics.

Video Modulator Kit $9.95

Convert your TV set into a high quality monitor without affecting normal usage. Complete kit with full instructions.

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1978 IC Update Master Manual **$30.00**
Complete IC data selector 2175 pg. Master reference guide. Over 42,000 cross references. Free update service through 1978. Domestic postage $3.50. Foreign $6.00. Final 1977 Master closeout **$15.00**

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Batt. oper. 1mV and .1NA resolution. Resistance to 20 meg. 1% accuracy. Small, portable, completely assem. in case. 1 yr. guarantee. **$59.95**

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100 pcs of 3" at $.82 = 3¼¢/ft.
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50 ft roll at $1 99 = 4¢/ft.
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30 Kynar stripped 1" on each end. Lengths are overall
Colors Red, Blue, Green, Yellow, Black, Orange, White
Wire packaged in plastic bags. Add 25¢/length for tubes

	100	500	1000	5000
2½ in	78	2 40	4 30/K	3 89/K
3 in	82	2 60	4 71/K	4 22/K
3½ in	86	2 80	5 12/K	4 55/K
4 in	90	3 00	5 52/K	4 88/K
4½ in	94	3 21	5 93/K	5 21/K
5 in	98	3 42	6 34/K	5 52/K
5½ in	1 02	3 65	6 75/K	5 86/K
6 in	1 06	3 85	7 16/K	6 19/K
6½ in	1 15	4 05	7 57/K	6 52/K
7 in	1 20	4 25	7 98/K	6 85/K
7½ in.	1 25	4 45	8 39/K	7 18/K
8 in	1 29	4 65	8 80/K	7 53/K
8½ in	1 32	4 85	9 21/K	7 84/K
9 in	1 36	505	9 62/K	8 17/K
9½ in	1 40	5 25	10 03/K	8 50/K
10 in	1 45	5 51	10 44/K	8 83/K
Addl. inches	10	41	82/K	66/K

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# 1	$6.95			# 2	$19.95				
250	3"	100	4½"	250	2½"	250	4½"	250	6"
250	3½"	100	5"	500	3"	250	5"	100	6½"
100	4"	100	6"	500	3½"	100	5½"	100	7"
				500	4"	1 250 ft	Roll Bulk		

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8pin*	41	38	35	31	29	27
14pin*	42	39	36	32	29	27
16pin*	46	43	39	35	32	30
18pin*	63	58	54	47	44	.41
20 pin	84	78	71	63	59	54
22pin*	1 30	1 20	1 10	95	90	.84
24 pin	91	84	78	68	64	59
28 pin	1 25	1 15	1 08	95	89	82
40pin	1 65	1 55	1 42	1 25	1 15	1 09

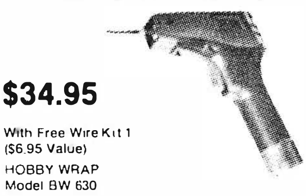
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All prices include gold
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Ribbon cable connectors for connecting boards to front panels, or board to board

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	14 pin	16 pin	24 pin	14 pin	16 pin	24 pin
6"	1 24	1 34	2 05	2 24	2 45	3 37
12"	1 33	1 44	2 24	2 33	2 55	3.92
24"	1 52	1 65	2 63	2 52	2 76	4 31
48"	1 91	2 06	3 40	2 91	3 17	5 08

WIRE WRAP TOOLS



$34.95

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Batteries & Charger	$11.00
WSU 30 Hand Wrap-Unwrap Strip Tool	5.95
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BT 30 Extra Bit	2.95

WIRE WRAP BOARDS

				1-4	5-9	10-24	WW Connector
H-PCB 1	4x4½	44	Buses on both sides	4.75	4.50	4.00	3.00
3662	4x6	44	Blank	6.25	5.85	5.50	3.00
3682	4x10	44	Buses on one side	10.50	10.00	9.50	3.00
3682-2	4x6	44	Buses on one side	9.50	9.00	8.25	3.00
4066-4	4x6	72	Buses on both sides	13.50	13.00	12.50	4.00
3719-1	4x6	72	Blank	9.00	8.50	8.00	4.00
3719-4	4x10	72	Blank	11.00	10.50	10.00	4.00
4350	7x9½	80	Buses on both sides	17.50	16.50	16.00	7.00
8800V	10x5.3	100	Buses on both sides	19.50	17.96	16.95	5.00
169P84	8½x17	–	Blank	6.25	5.75	5.25	–

SOCKET SALE!

	1-9	10-49	50 up
14 pin Gold WW	.34	.32	.30
16 pin Gold WW	.36	.35	.33
24 pin Gold WW	.75	.70	.68

Prices good through
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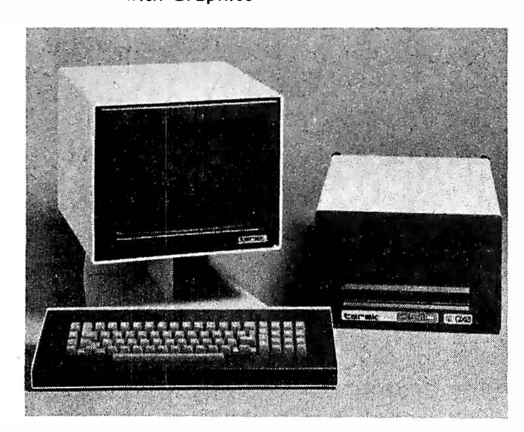
135 E. Chestnut Street 4A
Monrovia, California 91016
Phone (213) 357-5005

Circle 297 on inquiry card.

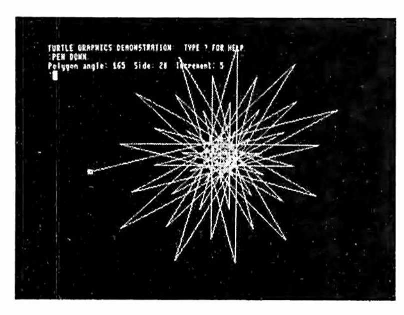
What's New?

SYSTEMS

A Complete PASCAL System with Graphics

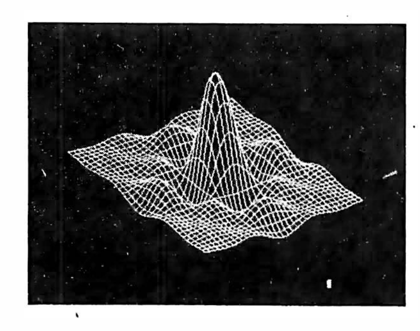


Over Christmas we had a chance to see this state of the art hardware and software system in action at the University of California, San Diego. It features a complete PASCAL based programming system running on an LSI-11 microcomputer with extensive graphics capabilities. The computer is a Terak 8510/a with 56 K bytes (28 K 16 bit words) of memory, a floppy disk drive and a disk controller which handles up to four drives, video control circuitry and an integral power supply. The display is a 12 inch diagonal P4 phosphor black and white monitor with a two inch speaker, and the 71 key keyboard features the full 128 character ASCII set plus a cursor control group and numeric key-

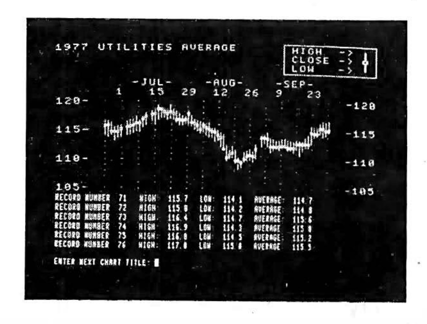


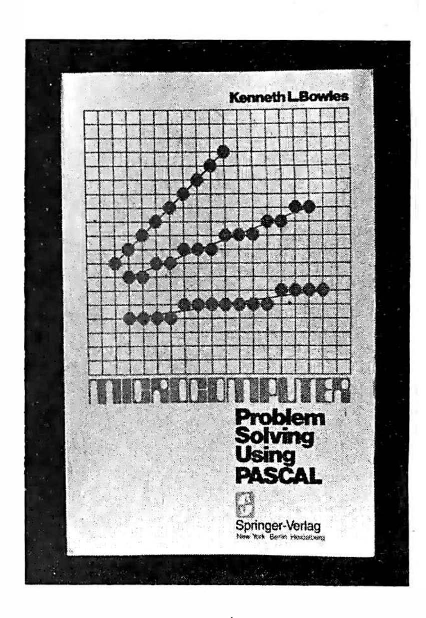
pad. 24 lines of 80 characters are displayed on the monitor from a 192 character code set defined by dot patterns in user alterable memory, so that foreign language, APL, and primitive graphics symbols can be displayed. Each character block is an 8 by 10 dot matrix, while graphics patterns can be generated from a bit mapped memory with 320 horizontal by 240 vertical point resolution. Horizontal and vertical dot spacing is identical, so that dimensional scaling of graphics patterns is simplified. Character and graphics dot matrices overlap yet are visually distinct, so both can be displayed simultaneously. Three horizontal blanking zones are available in both character and graphics displays, and continuous motion panning of the text display is possible. Software available with the system includes a macroassembler, single and multiple user BASIC, FORTRAN IV, APL and PASCAL.

The PASCAL system was developed at the UCSD Institute for Information Systems under the direction of Dr Kenneth Bowles, and includes a compiler for full PASCAL with graphics extensions, a text editor and text output formatter, a debugger, and a disk file management system with a command language. All this software is written in PASCAL and is translated into a very compact pseudocode which features frequency based encoding of the pseudo-



instruction set, so that the PASCAL compiler, for example, runs in 28 K words of memory. Only the pseudocode interpreter need be rewritten to make the system run on another microcomputer, and Bowles and his colleagues reportedly also have PASCAL implementations for the 8080 and Z-80 up and running. Another part of the package is a computer assisted instruction system consisting of tests and exercises running on the Terak 8510/a and written in PASCAL, which is used each term by several hundred students in the introductory programming course at UCSD. The textbook for this course, entitled *Microcomputer Problem Solving Using PASCAL*, was written by Bowles and produced, both text and graphics, on the PASCAL system. It emphasizes structured programming concepts which are expressed quite naturally in PASCAL, and illustrates PASCAL programming features with examples in graphics and text processing. PASCAL's





special features, such as its data structures, dynamic storage, set variables and recursion turn out to be surprisingly useful and practical in many of these applications. The Terak 8510/a, which is priced at $7850 with substantial discounts for educational institutions which are members of the EDUCOM consortium, is available from Terak Corp, 14425 N Scottsdale Rd, Suite 100, Scottsdale AZ 85260, (602) 991-1580; all software for the system is priced separately. The UCSD PASCAL system is available for a distribution fee of $200 from the Institute for Information Systems, Mail Code C-021, University of California at San Diego, La Jolla CA 92093, (714) 452-4526. The textbook *Microcomputer Problem Solving Using PASCAL* is available for $9.80 per copy from Springer-Verlag, 175 Fifth Av, New York NY 10010, (212) 477-8200. . .Dan Fylstra■

Circle 597 for Terak.
Circle 598 for UCSD PASCAL.
Circle 599 for Springer-Verlag.

Attention Readers, and Vendors. . .

Where Do New Product Items Come From?

The information printed in the new products pages of BYTE is obtained from "new product" or "press release" copy sent by the promoters of new products. If in our judgment the neat new whiz-bang gizmo or save the world software package is of interest to the personal computing experimenters and homebrewers who read BYTE, we print the information in some form. We openly solicit such information from manufacturers and suppliers to this marketplace. The information is printed more or less as a first in first out queue, subject to occasional priority modifications.

California Industrial

Post Office Box 3097 B • Torrance, California 90503



Diablo PRINTER



PRINTER ONLY! Keyboard models NOT available.

In February, when this advertisement was submitted to the publisher, we were negotiating for the purchase of several hundred used Diablo Terminals.

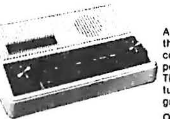
If we are successful in acquiring these units, they will be available in late April for only $850.00. FOB Los Angeles.

All terminals were removed from service in operating condition.

Word processing quality

ELECTRONIC ENTERTAINMENT CENTER

Tennis·Handball Hockey·Smash



Action-packed color entertainment for the whole family. Adjustable skill level controls allow players of all ages to compete in tennis, hockey and handball. This four game entertainment center turns your television into a video playground.

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New from Teletype, the Model 43 is capable of printing 132 ASCII characters per line. Send and receive data at 10 or 30 char. per second. Keyboard generates all 128 ASCII code combinations. RS-232 interface, same as the popular Model 33. Data sheet sent upon request. Manufacturer suggested price $1377.00.

IMMEDIATE DELIVERY $1219

TTL model with NOVATION brand Acoustic Modem. $1419

TELETYPE

HEXADECIMAL KEYBOARD

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Maxi-Switch hexadecimal keyboards are designed for microcomputer systems that require 4-bit output in standard hexcode.

Each assembly consists of 16 hermetically sealed reed switches and TTL "one shot" debounce circuitry.

Reliable lowfrictionacetal resin plungersarecredited forthe smooth operation and long life of this premium keyboard.

Requires single +5 voltsupply.



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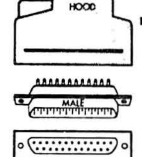


Walnut-grained decorator clock features large .7" LED display which is driven by the new National MM5385 alarm clock chip. Preset 24-hour alarm function allows you to awaken at the same time each morning without resetting. Upon reaching the wake-up time, the clock's loudspeaker emits a gentle tone. Touch the snooze button and doze off for an additional 9 minutes of sleep. Clock also functions as a ten-minute elapse timer. "Alarm Set" indicator, AM-PM display.

CONNECTORS

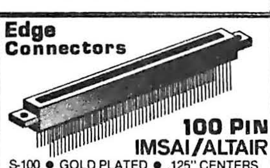
your choice **DB25P** male plug & hood or **DB25S** female

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Qty.	fe.	male	hd.
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25	3.15	2.25	1.05
100	2.85	1.90	.95
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Edge Connectors



100 PIN IMSAI/ALTAIR

S-100 • GOLD PLATED • .125" CENTERS

Altair .140 row, soldertail. . . . . $5.98 3/$16.50
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SPECIALS

W/W same as above without ears$3.50 3/$10
72 (dual 36) W/W .156" centers. . . $2.50 3/$6



$24.88

SPERRY UNIVAC KEYBOARD

The famous Sperry Univac 1710 Hollerith keyboard assembly is now available from California Industrial for only $24.88. The ideal computer input device for accountants and mathematicians. The numeric keys are placed on the lower three rows to resemble a ten key adding machine. This format allows one handed numeric data entry. Original cost was $385. Used but guaranteed in excellent condition. Complete with documentation.

Quiet Buss™ S-100 MOTHER

The Quiet Buss from California Industrial is quality engineered. No short cuts have been taken to produce this mother board. Active termination circuitry prevents noise and crosstalk. Manufactured from extra heavy FR-4 epoxy glass. Features 2 ounce double thicknesscopper traces.

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Ideal for analoginterface systems sucrias Southwest, Tarbell and the Commodore Pet.

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Please specify IBM 3740 series or 32 sector.

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Certified Digital CASSETTES Won't drop a BIT!

$5.50



CALIFORNIA INDUSTRIAL is an Authorized Dealer of Scotch Brand Data Products

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This joystick feature four 100K potentiometers, that vary resistance proportional to the angle of the stick. Perfect for television games, quad stereo and radio controlled aircraft.

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8K UV Erasable MEMORY

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GP100-Maximum design versatility along with standard address decoding and buffering for S100 systems. Room for 32 uncommitted 16 pin IC's, 5 bus buffer & decoding chips, 1 DIP address select switch, a 5 volt regulatorandmore.

WW100-Wire wrap breadboard, similar tothe GP100. Allows wire wrap of all sizes of sockets in any sizes of sockets in any combination. An extra regulator position for multiple voltage applications.



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7410	.19
7411	.25
7412	.35
7413	.49
7414	.79
7416	.39
7417	.39
7420	.19
7422	.49
7423	.39
7425	.39
7426	.39
7427	.39
7428	.49
7429	.39
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GENERAL INSTRUMENT ASCII Keyboard Encoder AY 5-3600 Prime but house marked only $4.95

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The Atari R.F. Modulator allows computer data to be displayed directly upon your existing television system. This unit converts the signal from the Apple II and other video sources into television frequencies. Operates from single 5 volt supply. Complete with metal case, mating R.F. connector and 15 feet of coax cable. Schematics and instructions included.



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20	50	100
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Coil 12 Volt dc.
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2N3906	.15	.11	.09	.07

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Heavy duty grounded power cord and mating chassis connectors.



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Battery wire wrapping tool

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OK HOBBY WRAP-30 wire wrap & strip tool **$5.45**

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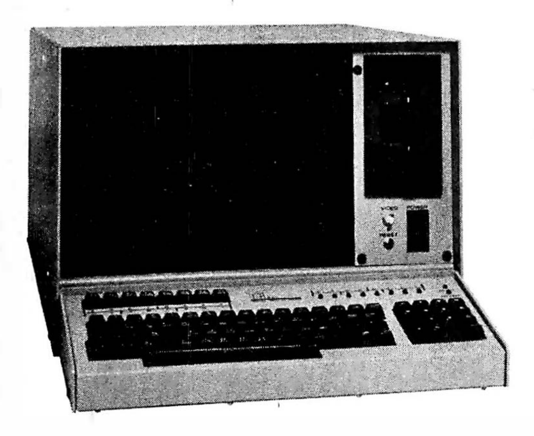
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VISA



Circle 37 on inquiry card.

A High End "Appliance" Computer



A self-contained desktop computer with floppy disk drive and systems software is now being marketed by CMC Marketing Corp, 5601 Bintliff, Suite 515, Houston TX 77036. The system, manufactured by TEI Inc, is based on the Altair (S-100) bus design and includes the following key items:

- 8080 central processor
- 32 K static programmable memory
- disk controller capable of handling three drives
- one Shugart SA-400 minifloppy disk drive
- three parallel eight bit data ports
- three serial data ports with selectable rates from 75 to 9600 bps, RS-232 or TTL levels.
- video display with 24 lines of 80 characters using a 15 inch diagonal high resolution monitor
- ASCII keyboard with eight special function keys for user definitions, and numeric keypad
- CP/M operating system and a 20 K BASIC interpreter

The model MCS-PT112/32 comes fully assembled and tested at a price of $4795.■

Circle 601 on inquiry card.

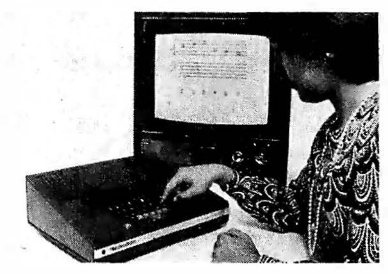
Complete Business System Under $10,000



The INFO 2000 Business System, said to compete in performance and capability with minicomputer systems selling for $30,000 or more, employs the Altair (S-100) bus with a Z-80 processor, up to 56 K of user memory, 8 K of read only memory, a filtered forced air cooling system and a heavy duty power supply. Mass storage is provided with Persci dual flexible disk drives. The printer, which operates at 160 characters per second, provides 132 columns of 95 ASCII upper and lower case alphabetic and graphic characters. The video terminal features dual display intensity, protected fields and 19,200 bps operation. Business application software includes CPA 2000, an accounting package, TEXT 2000, a word processing package, and a disk operating system. Optional software includes a disk BASIC, ANSI FORTRAN, a macro assembler, text editor, debugger and utilities. Planned are the PAY 2000 payroll system and the STOCK 2000 inventory control system. More details are available from INFO 2000 Corp, 20630 S Leapwood Av, Carson CA 90746, (213) 532-1702.■

Circle 600 on inquiry card.

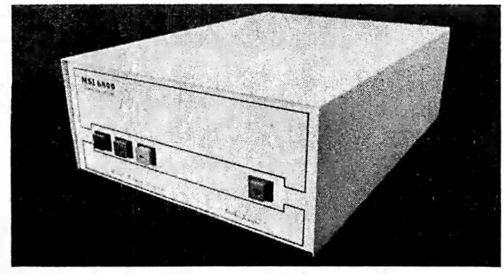
Consumer Oriented Computer Comes with Program Library



Aimed at the average consumer, the VideoBrain computer comes with a preprogrammed library of entertainment, education and home management applications on plug in cartridges. Based on the F8 microprocessor, the basic unit includes 4 K bytes of read only memory and 1 K bytes of programmable memory, while the plug in cartridges can contain up to 13 K bytes of read only or programmable memory. The VideoBrain is designed to connect to a home color television set and comes with an AC adapter, TV hookup cord, antenna switch box, two joysticks, and three introductory cartridges. The typewriter style keyboard includes 36 keys capable of producing 71 distinguishable input symbols, while the video output circuits provide sound and picture signals for the TV set. The programs which come with the system in read only memory allow the user to type and edit a message of seven lines and 16 characters per line, change the color of the screen or the size of the letters, examine a clock and calendar, or preset an alarm which will sound on the TV set at the appropriate time and display the stored message. Twelve plug in cartridges are currently offered: Finance, Cash Management, Stock Valuation, Real Estate, Music Teacher, Math Tutor, two Wordwise programs, Gladiator, a game with 384 variations, Blackjack, Checkers and Pinball. Over 50 programs are under development and will be released over the coming year. The VideoBrain will be sold through department stores and specialty electronic stores at a suggested retail price of $500, and is made by Umtech Inc, 150 S Wolfe Rd, Sunnyvale CA 94086, (408) 737-2680.■

Circle 629 on inquiry card.

More Capabilities in This New 6800 System



The MSI 6800 computer system offers additional memory and interfacing capabilities using the SwTPC (SS-50) bus. Its power supply delivers 20 A at 5 V and 3 A at 15 V to support up to 56 K bytes of memory, using either 110 V 60 Hz or 220 V 50 Hz line current. The motherboard provides 16 slots for full size system boards, and an interface adapter board (with eight slots) must be used to accommodate smaller interface boards. The processor board includes sockets for 4 K bytes of programmable read only memory and separate system and serial data rate clocks. An ACIA is used for the standard serial device interface. The MSIBUG system monitor, supplied in read only memory, offers flexible memory examine and change, register dump and instruction list, and terminal IO control functions. All memory addresses are fully decoded, with only the upper 8 K bytes of the address space used for the system and extended monitors. Full modem control functions are supported on the MSI serial interface board. The MSI 6800 measures 20 by 16 by 7 inches and is supplied with 8 K bytes of user memory, the interface adapter and serial interface boards for $595 in kit form or $895 assembled and tested, from Midwest Scientific Instruments, 220 W Cedar, Olathe KS 66061.■

Circle 630 on inquiry card.

New!

16K E-PROM CARD

IMAGINE HAVING 16K OF SOFTWARE ON LINE AT ALL TIME!

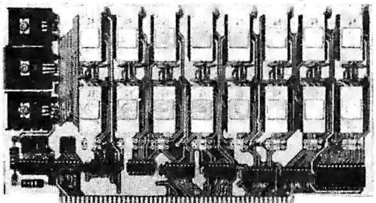
S-100 (Imsai/Altair) Buss Compatible!

Uses 2708's!

KIT FEATURES:

1. Double sided PC board with solder mask and silk screen and gold plated contact fingers.
2. Selectable wait states.
3. All address lines & data lines buffered!
4. All sockets included.
5. On card regulators.

KIT INCLUDES ALL PARTS AND SOCKETS (except 2708's). Add $25. for assembled and tested.



DEALER INQUIRIES INVITED!

PRICE CUT!

$57.50 kit

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SPECIAL OFFER:

Our 2708's (450NS) are $12.95 when purchased with above kit.

Fully Static!



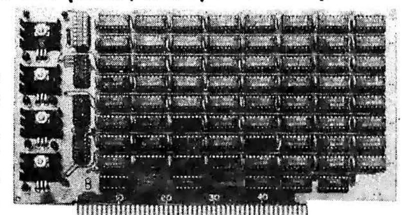
S-100 (Imsai/Altair) Buss Compatible!

ADD $20 FOR 250NS

KIT FEATURES:

1. Doubled sided PC Board with solder mask and silk screen layout. Gold plated contact fingers.
2. All sockets included.
3. Fully buffered on all address and data lines.
4. Phantom is jumper selectable to pin 67.
5. FOUR 7805 regulators are provided on card.

(450NS)



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Fully Assembled & Burned In
$179.00
Blank PC Board w/ Documentation
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Support IC's (TTL & Regulators)
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MC 3401. PIN FOR PIN SUB. FOR POPULAR LM 3900.
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ALARM CLOCK CHIP
N.S. MM5375AA. Six Digits. With full Data. **New!**
$1.95 each

FULL WAVE BRIDGE
4 AMP. 200 PIV.
69¢ EA. 10 FOR $5.75

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MOTOROLA 7805R VOLTAGE REGULATOR
Same as standard 7805 except 750 MA output. TO—220. 5VDC output.
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Now full speed! Prime new units from a major U.S. Mfg. 450 N.S. Access time. 1K x 8. Equiv. to 4-1702 A's in one package.
$15.75 ea. Special Offer: $12.95 each when purchased with our 16K EPROM kit!

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By Mostek, The major Z-80 second source. The most detailed explanation ever on the working of the Z-80 CPU CHIPS. At least one full page on each of the 158 Z-80 instructions. A MUST reference manual for any user of the Z-80. 300 pages. Just off the press! A D.R.C. exclusive! $12.95

CMOS SPECIAL!
CD 4001 – 5 for $1.
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CD 4013 – 3 for $1.
CD4040 – $1. each
CD4042 – 2 for $1.
CD 4049 – 3 for $1.

POWER RECTIFIER #2 Motorola
Stud Mount. 1N1187.
35 AMPS. 300 PIV.
Military Quality! $1.19 ea. or 4/$3.50

3 AMP RECTIFIER
1N4721. Axial Lead. 200 PIV.
HEAVY DUTY!
House numbered
4 for $1.00 Metal Case

4K STATIC RAM'S
2114. The new industry standard. Arranged as 1K x4. Equivalent to 4-21 L02's in 1 package! 18 pin DIP. 2 chips give 1Kx8.
2/$24. 8/$85.

OPCOA LED READOUT
SLA-1. Common Anode. .33 inch character size. The original high efficiency LED display. 75c ea. or 4 for $2.50

EXPERIMENTER'S CRYSTAL
262.144KHZ. This frequency is 2 to the 18th power. Easily divided down to any power of 2, and even to 1HZ. New by CTS-Knight. A $5. value!
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3 Cell pack, gives 4 volts at 900MAH. Brand new, factory fresh. Each cell is 2/3 "C" size. $4.50 /pack. Buy 3 packs (12 volts) for $10.95. Limited stock!

741C OP AMPS
Mini Dip. Prime new units. Has computer Mfg's house number.
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.1 MFD 16V. P.C. leads. Most popular value. By Sprague.
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GE 10 AMP Triac
SC146D. House no. To-220 case. Rated 10 amps 400PIV.
75cea. 3/$2.

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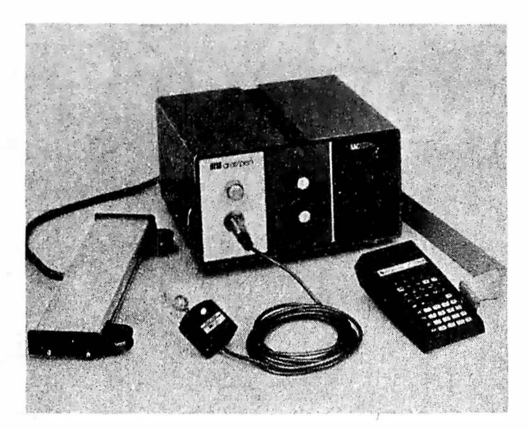
74LS00 — 33c	74LS74 — 49c
74LS02 — 35c	74LS90 — 69c
74LS04 — 35c	74LS138—89c
74LS08 — 35c	74LS154—1.49
74LS10 — 33c	74LS175—1.10
74LS20 — 33c	74LS367—75c
74LS73 — 49c	74LS368—85c

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Circle 100 on inquiry card.

Digitizer Input for the SR-52 Calculator



This digitizer, a first in peripherals for programmable calculators, is designed to eliminate manual entry of graphical data to the calculator, saving time, hand calculations and transcription errors. The GP-352 consists of the basic Graf/Pen Model GP-3 sonic digitizer, a Texas Instruments SR-52 calculator, and the necessary interface, cabling, and plug in connector. The interface simulates the action of pressing keys on the calculator to provide data input. Although the resulting system is somewhat slower than other digitizers, the user gains the advantage of the large library of application programs available from TI. The manufacturer also operates a telephone hotline and will write custom programs for users. The sonic digitizer includes a 14 inch aluminum data tablet, stylus or cursor, and control unit. A moveable NT-Series sensor bar may be used in place of the data tablet, and standard sizes larger than 14 inches are also available. The GP-352 system, which includes the calculator, is priced at $2850. Customers may provide their own calculators, but the manufacturer will honor the Texas Instruments warranty only for calculators which it supplies. Also planned is the GP-359 for the TI 59 calculator. More information is available from Science Accessories Corp, 970 Kings Highway W, Southport CT 06490, (203) 255-1526.■

Circle 593 on inquiry card.

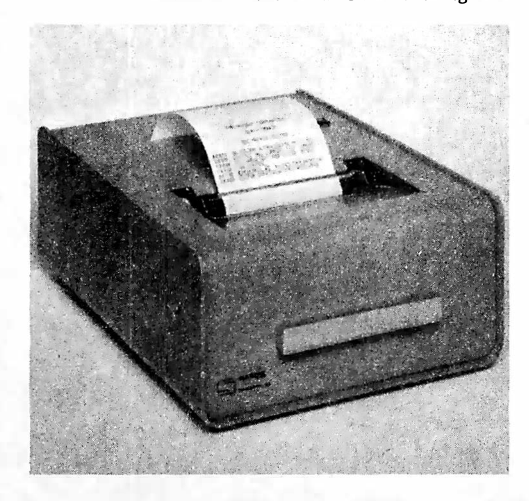
Text Editing System Fits Inside Selectric



The Transwriter is housed entirely within an unaltered Selectric II correcting typewriter and uses "memory wafers" as its storage media. Each wafer measures about 2 by 1 by 0.2 inches and stores up to 20 typewritten pages. The unit's text editing features include automatic tabbing, stop codes, automatic lift off correction and format stored with the text, and the ability to insert an unlimited amount of new text. The Transwriter, which will be sold through local office machine dealers at a list price of $2995, is offered by Transaction Data Systems, 2909 Oregon Ct #C-6, Torrance CA 90503, (213) 624-3213.■

Circle 594 on inquiry card.

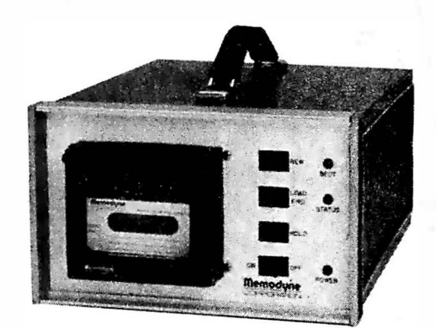
40 Column Printer Has Some Intelligence



The SP-302 Digital Printer uses a microprocessor controller to add some "intelligence" to its printing functions. Special features include double width printing, double and triple spacing, and standard tab functions for simple software control from a host device or computer. The device prints alphabetic and numeric information in 40 characters per line at speeds up to 50 characters per second, with multiple copy capability. An RS232 and 20 mA current loop interface are included, with a standard data rate of 110 bps. Other data rates as well as the printing intensity can be set with internal jumpers. The SP-302 is $575 in single quantities from Syntest Corp, 169 Millham St, Marlboro MA 01752, (617) 481-7827.■

Circle 595 on inquiry card.

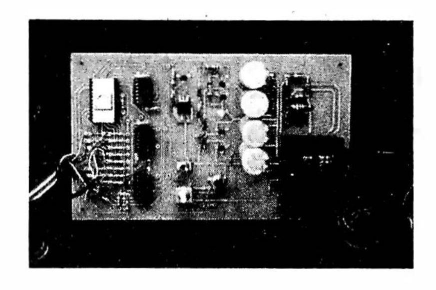
Offline Recorder for Silent 700



The Memodyne ANSI Compatible Recording System Model 2146 is a compact write only recorder designed to record offline at remote sites and times to free up a terminal. It accepts serial data at five selectable data rates from 110 to 1200 bps and records in ANSI and ECMA format at 800 bits per inch. It will also accept parallel data. Standard Philips cassettes are used. The unit will play back directly on a Texas Instruments Silent 700 terminal or on a Memodyne 3765-8 recorder. The Model 2146 includes front panel controls, input and output connectors, power supplies and a carrying case, measures 10.5 by 7 by 11.5 inches and weighs ten pounds. It sells for $1725 with quantity discounts available from Memodyne Corp, 385 Elliott St, Newton MA 02164, (617) 527-6600.■

Circle 596 on inquiry card.

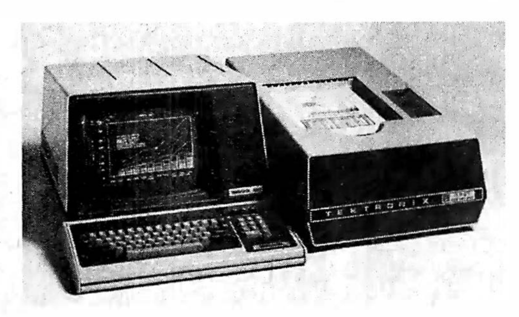
2704/2708 EROM Programmer



The EPB-2 Programmer for 2704/2708 EROMs has been developed by F & D Associates, 1210 Tood Rd, New Plymouth OH 45654. The unit uses software for its timing and control functions. All components, including power supply, fit on one 5 inch by 8 inch printed circuit board. The unit was primarily designed for the SwTPC 6800 but, according to the manufacturer, can be easily adapted to the IO ports of other microprocessors. The software provided is written for a SwTPC 6800 microcomputer system using a Teletype or TV type interface operating with the MIKBUG monitor. To facilitate customizing or adapting to other systems, it is written in short subroutines and a source listing is supplied. The bare board, software and documentation is available at $29 plus $2.50 shipping. Documentation only is available at $5 postpaid refundable with order.■

Circle 608 on inquiry card.

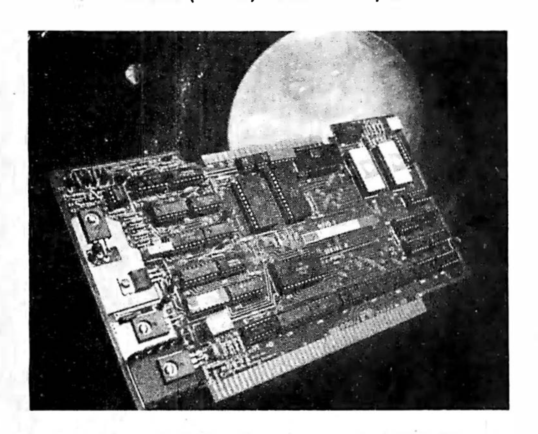
Terminal Features Character Level Mapping of Graphics



The 4025 display terminal represents graphics patterns in its internal memory on a character by character basis rather than as a bit map for all the points on the screen. Each character area, an 8 by 14 dot matrix, can display either an alphanumeric character or the pattern of dots represented by a bit map of that character position. Thus less memory is required to represent a graph that fills only part of the screen, and graphs can be scrolled up the screen along with alphanumeric characters. The 4025's display screen provides 34 lines of 80 characters each, or 640 by 480 addressable points for graphing purposes. 30 pages of 34 lines with an average of 20 characters per line can be stored in the terminal's internal 32 K byte memory. The graphics memory can also be used to define additional character fonts which can be sent to the terminal from the host computer. Commands from the computer to the terminal are represented by "English language" ASCII strings instead of special codes, and may be intermixed with display information. Graphics plotting packages are available for implementation on the host computer. The 4631 copier, which can copy up to 53 80 character lines or graphics patterns on an 8.5 by 11 inch sheet of paper, can be attached to the 4025 display controller. The 4025 is available at a base price of $3595 with a wide variety of expansion options from Tektronix Inc, POB 500, Beaverton OR 97077, (503) 644-0161.■

Circle 631 on inquiry card.

Altair (S-100) General Purpose IO Board

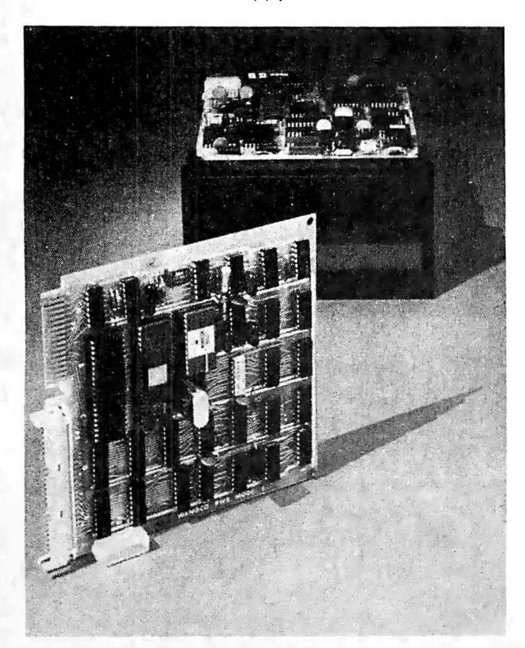


Infinite Incorporated, 1924 Waverly Pl, Melbourne FL 32901, has announced the MFIO-1, an Altair (S-100) compatible general purpose IO board. The board features a memory or IO mapped parallel input port for keyboard, memory or IO mapped serial IO port with crystal controlled switch selectable data rates of 50 to 19200 bps, jumper selectable RS 232 or 20 mA current loop, memory or IO mapped cassette interface with switch selectable data rates of 300 (Kansas City Standard), 600, 1200 and 2400 bps, 128 bytes of programmable scratchpad memory, and slots for two 2708 erasable read only memories. A 21 command, 2 chip monitor program is available in read only memory. Total power requirement is less than 1 A.

The MFIO-1 is being made available in three versions, assembled and tested ($282), complete kit ($234), and bare boards ($65.95).■

Circle 632 on inquiry card.

Smart Minifloppy Controller Uses Intel 8084



The 8201 Micro-Controller provides a general purpose minfloppy disk drive interface for byte oriented computer systems. One version of the 8201 is pin compatible with the Altair (S-100) bus. The interface features an Intel 8048 microcomputer on a chip which supports nine commands from the host computer system. The 8201 will perform soft sectored formatting with 16 sectors per track and 128 bytes per sector. It can control up to four drives and will duplicate information from one drive to another upon a single command from the host system. A diagnostic command is also included. The interface is built on a printed circuit board which can be mounted on top of a minifloppy disk drive. The 8201 is priced at $490 in single quantities with OEM discounts available from Wangco Inc, a division of Perkin-Elmer Data Systems, 5404 Jandy Pl, Los Angeles CA 90066, (213) 390-8081.■

Circle 633 on inquiry card.

North Star Now Offers Terminal for Horizon



North Star Computers has introduced a 24 line by 80 character video display terminal marketed for use with their Horizon computer.

The CRT terminal is manufactured by Soroc Technology, and can be connected to the Horizon with data rates up to 9600 bps. The terminal is the Soroc model IQ 120 with an addressable cursor, upper and lower case ASCII character set and a numeric key pad. A 90 day limited warranty is honored by Soroc.

The North Star Horizon computer is a disk oriented computer with a 4 MHz Z-80 A processor, 12 slot Altair (S-100) motherboard, 16 K byte programmable memory, one or two Shugart minifloppy disk drives and the serial IO interface which talks to the terminal.

The Soroc IQ 120 Terminal is $995 fully assembled.

Delivery is quoted as stock to 90 days, and the terminal is available at local North Star dealers. North Star Computers Inc is located at 2547 Ninth St, Berkeley CA 94710. A 16 page catalog detailing North Star products is also available on request.■

Circle 634 on inquiry card.

What's New?

Compac Introduces Programming Aides

BASE CONVERSION TABLE

BIN	OCT	DEC	HEX	2's COMP	BIN	OCT	DEC	HEX	2's COMP
0	0	0	00	0	1000000	100	64	40	64
1	1	1	01	1	1000001	101	65	41	65
10	2	2	02	2	1000010	102	66	42	66
11	3	3	0	3	1000011	103	67	43	67
100	4	4	04	4	1000100	104	68	44	68
101	5	5	05	5	1000101	105	69	45	69
110	6	6	06	6	1000110	106	70	46	70
111	7	7	07	7	1000111	107	71	47	71
1000	10	8	08	8	1001000	110	72	48	72
1001	11	9	09	9	1001001	111	73	49	73
1010	12	10	0A	10	1001010	112	74	4A	74
1011	13	11	0B	11	1001011	113	75	4B	75
1100	14	12	0C	12	1001100	114	76	4C	76
1101	15	13	0D	13	1001101	115	77	4D	77
1110	16	14	0E	14	1001110	116	78	4E	78
1111	17	15	0F	15	1001111	117	79	4F	79
10000	20	16	10	16	1010000	120	80	50	80
10001	21	17	11	17	1010001	121	81	51	81
10010	22	18	12	18	1010010	122	82	52	82
10011	23	19	13	19	1010011	123	83	53	83
10100	24	20	14	20	1010100	124	84	54	84
10101	25	21	15	21	1010101	125	85	55	85
10110	26	22	16	22	1010110	126	86	56	86
10111	27	23	17	23	1010111	127	87	57	87
11000	30	24	18	24	1011000	130	88	58	88
11001	31	25	19	25	1011001	131	89	59	89
11010	32	26	1A	26	1011010	132	90	5A	90
11011	33	27	1B	27	1011011	133	91	5B	91
11100	34	28	1C	28	1011100	134	92	5C	92
11101	35	29	1D	29	1011101	135	93	5D	93
11110	36	30	1E	30	1011110	136	94	5E	94
11111	37	31	1F	31	1011111	137	95	5F	95
100000	40	32	20	32	1100000	140	96	60	96
100001	41	33	21	33	1100001	141	97	61	97
100010	42	34	22	34	1100010	142	98	62	98
100011	43	35	23	35	1100011	143	99	63	99
100100	44	36	24	36	1100100	144	100	64	100
100101	45	37	25	37	1100101	145	101	65	101
100110	46	38	26	38	1100110	146	102	66	102
100111	47	39	27	39	1100111	147	103	67	103
101000	50	40	28	40	1101000	150	10	68	104
101001	51	41	29	41	1101001	151	105	69	105
101010	52	42	2A	42	1101010	152	106	6A	106
101011	53	43	2B	43	1101011	153	107	6B	107
101100	54	44	2C	44	1101100	154	108	6C	108
101101	55	45	2D	45	1101101	155	109	6D	109
101110	56	46	2E	46	1101110	156	110	6E	110
101111	57	47	2F	47	1101111	157	111	6F	111
110000	60	48	30	48	1110000	160	112	70	112
110001	61	49	31	49	1110001	161	113	71	113
110010	62	50	32	50	1110010	162	114	72	114
110011	63	51	33	51	1110011	163	115	73	115
110100	64	52	34	52	1110100	164	116	74	116
110101	65	53	35	53	1110101	165	117	75	117
110110	66	54	36	54	1110110	166	118	76	118
110111	67	55	37	55	1110111	167	119	77	119
111000	70	56	38	56	1111000	170	120	78	120
111001	71	57	39	57	1111001	171	121	79	121
111010	72	58	3A	58	1111010	172	122	7A	122
111011	73	59	3B	59	1111011	173	3	7B	123
111100	74	60	3C	60	1111100	174	124	7C	4
111101	75	61	3D	61	1111101	175	125	7D	125
111110	76	62	3E	62	1111110	176	126	7E	126
111111	77	63	3F	63	1111111	177	127	7F	7

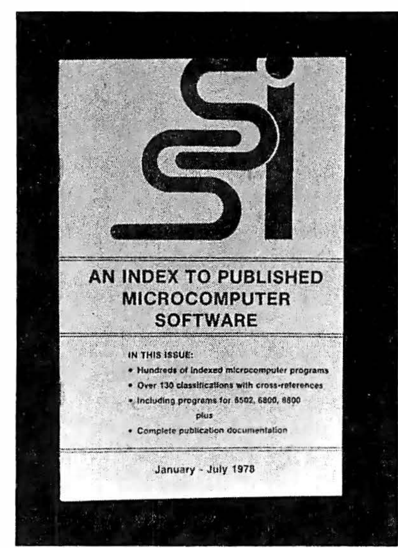
The Base Conversion Table enables the programmer to easily look up the representation of decimal numbers 0 to 255 in binary, octal, hexadecimal and two's complement bases. This table is tabulated in easy to read columns and prepunched for notebooks. Retail price is $2 each or $5 for three.

Another offering is a Coding Form, designed to be compatible with most microprocessing assembly language formats, which will organize and simplify your source code. Features include columns for labels, op codes and operands of source code; 50 sheets per pad and 25 lines per page; holes predrilled to match 3 ring binders. Retail price is $2.25 each or $6 for three.

Dealer inquiries are invited on both of these items. Contact Compac, POB 18470, Cleveland OH 44118.■

Circle 624 on inquiry card.

An Index to Published Microcomputer Software



How do you find that program you need today which you think you saw published in some personal computer magazine sometime in the last six months? You can avoid an exhaustive (and exhausting) search with the aid of the *Schreier Software Index*. The *SSI* indexes hundreds of published programs in over 130 categories, complete with cross references. Its sources include ten different personal computer magazines and nine compilations of programs in book form. Programs in BASIC as well as in machine language for the popular microprocessors are indexed so that, for example, finding a random number routine for the 8080 takes but a few seconds. The January to June 1978 issue of the *SSI* is printed on 5.5 by 8.5 inch enameled stock with a textured cover and should withstand repeated use. Future issues will be published biannually. The first issue is $4.95 from the Schreier Software Index, 4327 E Grove St, Phoenix AZ 85040.■

Circle 625 on inquiry card.

Catalog Describes Microcomputer Boards

This six page, 2 color brochure describes a broad line of microcomputer boards, printed circuit boards and off the shelf designer breadboards. Featured products include a 32 K byte static memory board, a general purpose board and a wire wrap board for the Altair (S-100) bus. The catalog also describes the technical capabilities of the manufacturing firm. Copies are free from Artec Electronics Inc, 605 Old County Rd, San Carlos CA 94070.■

Circle 627 on inquiry card.

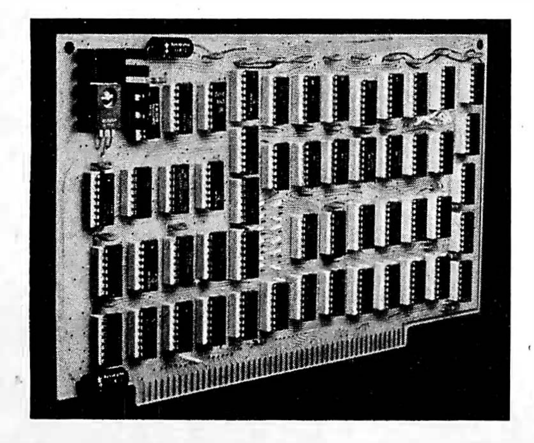
Stimulating Programs



Stimulating Simulations is a compilation of ten original simulation game programs in BASIC, designed both for entertainment and for self-education in programming concepts. It was written by Dr C William Engel, who is professor of mathematics education at the University of South Florida. The programs, such as Diamond Thief, Lost Treasure, Forest Fire and Space Flight, are written to be intriguing, yet comparatively easy to understand and modify. Each program comes with a complete source listing, sample run, user instructions, flowcharts, variables list and suggestions for major and minor modifications and improvements. The narrative text and illustrations serve to heighten the entertainment value of each game. The programs are written in MITS 8 K BASIC Version 3.2, and should be adaptable to similar BASICs. Special versions of the programs for the Commodore PET and and Radio Shack TRS-80 computers are also available on cassette. The book alone is $5 per copy from Engel Enterprises, POB 16612, Tampa FL 33687, (813) 988-3142, while the PET or TRS-80 cassette alone is $9.95, or $14.95 together with the book, from Personal Software, POB 136, Cambridge MA 02138, (617) 783-0694.■

Circle 628 on inquiry card.

Better Bug Trap



The Better Bug Trap is an Altair (S-100) bus compatible board providing functions for software debugging and real time processing. Four hardware breakpoints anywhere in memory detect all memory accesses, not just instruction fetches. Real time functions include time of day clock, interval timer, and watchdog timer. The Better Bug Trap generates its own interrupts and services them with a CALL instruction to a subroutine anywhere in memory. All functions, timing, breakpoints and subroutine addresses are set using software. Documentation includes a hardware manual with schematics, a software manual, and a software package for setting the board's functions.

The Better Bug Trap is assembled, tested, and delivered from stock for $180. A partial kit consisting of printed circuit board, voltage regulator, heat sink, and complete documentation is available for $45. A set of 52 integrated circuit sockets is $12. Contact Micronics Inc, POB 12545, Raleigh NC 27605.■

Circle 626 on inquiry card.

SOCKET JUMPERS

Mates with two rows of .025" sq. or dia. posts on patterns of .100" centers and shielded receptacles. Probe access holes in back. Choice of 6" or 18" length.

Part No.	No. of Contacts	Length	Price
924003-18R	26	18"	$ 5.38 ea.
924003-06R	26	6"	4.78 ea.
924005-18R	40	18"	8.27 ea.
924005-06R	40	6"	7.33 ea.
924006-18R	50	18"	10.31 ea.
924006-06R	50	6"	9.15 ea.

JUMPER HEADERS

Solder to PC boards for instant plug-in access via socket-connector jumpers. .025" sq. posts. Choice of straight or right angle.

Part No.	No. of Posts	Angle	Price
923863-R	26	straight	$1.28 ea.
923873-R	26	right angle	1.52 ea.
923865-R	40	straight	1.94 ea.
923875-R	40	right angle	2.30 ea.
923866-R	50	straight	2.36 ea.
923876-R	50	right angle	2.82 ea.

INTRA-CONNECTOR

Provides both straight and right angle functions. Mates with standard .10" x .10" dual row connectors (i.e. 3m, Ainsley, etc.) Permits quick testing of inaccessible lines.

Part No.: 922576-26 No. of contacts: 26 Price $6.90 ea.

INTRA-SWITCH

Permits instant line-by-line switching for diagnostic or QA testing. Switches actuated with pencil or probe tip. Mates with standard .10" x .10" dual-row connectors. Low profile design. Switch buttons recessed to eliminate accidental switching.

Part No.: IS-26 No. of contacts: 26 Price $13.80 ea.

CRYSTALS

THESE FREQUENCIES ONLY

Part #	Frequency	Case/Style	Price
CY1A	1.000 MHz	HC33/U	$5.95
CY2A	2.000 MHz	HC33/U	$5.95
CY2.01	2.010 MHz	HC33/U	$ .99
CY3A	4.000 MHz	HC18/U	$4.95
CY7A	5.000 MHz	HC18/U	$4.95
CY12A	10.000 MHz	HC18/U	$4.95
CY14A	14.31818 MHz	HC18U	$4.95
CY19A	18.000 MHz	HC18/U	$4.95
CY22A	20.000 MHz	HC18/U	$4.95
CY30B	32.000 MHz	HC18/U	$4.95

CONNECTORS

PRINTED CIRCUIT EDGE-CARD

.156 Spacing-Tin-Double Read-Out

Bifurcated Contacts — Fits .054 to .070 P.C. Cards

15/30	PINS (Solder Eyelet)	$1.95
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25 PIN-D SUBMINATURE (RS232)

DB25P	PLUG	$3.25
DB25S	SOCKET	$4.95
DB51226-1	COVER FOR 25S/25P	$1.75

LOTS OF POTS

Untested ⅜" square Spectrol Trimpots
Single-turn Printed Circuit Potentiometers

GB134	3 ea. of:	10-20-25-50 100-200-250-500 ohm	= 24 pcs.	$2.95
GB135	3 ea. of:	1K-2K-2.5K-5K 10K-20K-25K-50K	= 24 pcs.	$2.95
GB136	3 ea. of:	100K-200K-250K-500K 1Meg-2Meg-2.5Meg-5Meg	= 24 pcs.	$2.95

(Values subject to substitution within each group.)

'EXTRA SAVINGS' Buy all 3 (GB134, 135 & 136) for only $7.49

SWITCHES

¼" mounting holes

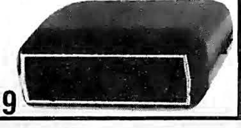
	Part			1-9	10+
TOGGLE (sub-miniature)	JMT121	SPDT	on-off-on	$1.95	$1.43
	JMT123	SPDT	on-none-on	1.65	1.21
	JMT221	DPDT	on-off-on	2.55	1.87
	JMT223	DPDT	on-none-on	2.15	1.58
TOGGLE (Printed Circuit)	MPC121	SPDT	on-off-on	$2.05	$1.53
	MPC123	SPDT	on-none-on	1.75	1.31
	MPC221	DPDT	on-off-on	2.65	1.97
	MPC223	DPDT	on-none-on	2.25	1.68
PUSH BUTTON	PB123	SPDT	maintained	1.95	1.47
	PB126	SPDT	momentary	1.95	1.47
PUSH BUTTON Miniature	MS102	DPST	momentary open	.35	.30
	MS103	SPST	momentary closed	.35	.30
DIPSWITCH SPST	206-4	8 pin dip	4 switch	1.75	1.65
	206-7	14 pin dip	7 switch	1.95	1.85
	206-8	16 pin dip	8 switch	2.25	2.15

1/16 VECTOR BOARD

	0.1" Hole Spacing Part No	P-Pattern L	W	Price 1-9	10 up
PHENOLIC	64P44 062XXXP	4.50	6.50	1.72	1.54
	169P44 062XXXP	4.50	17.00	3.69	3.32
EPOXY GLASS	64P44 062WE	4.50	6.50	2.07	1.86
	84P44 062WE	4.50	8.50	2.56	2.31
	169P44 062WE	4.50	17.00	5.04	4.53
	169P84 062WE	8.50	17.00	9.23	8.26
EPOXY GLASS COPPER CLAD	169P44 062WEC1	4.50	17.00	6.80	6.12

INSTRUMENT/ CLOCK CASE

Injection molded unit. Complete with red bezel. 4½" x 4" x 1-9/16".



$3.49

MICROPROCESSOR COMPONENTS

8080A	CPU	$10.95	Z80	CPU	$24.95
8212	8 Bit Input/Output	4.95	CDP1802	CPU	19.95
8214	Priority Interrupt Control	7.95	MC6800	8 Bit MPU	19.95
8216	Bi-Directional Bus Driver	4.95	MC6810AP1	128 x 8 Static RAM	5.95
8224	Clock Generator/Driver	5.95	MC6820	Periph. Interface Adapter	7.95
8228	System Controller Bus Driver	5.95	MC6830L8	1024 x 8 Bit ROM	14.95

CPU'S

8080A	Super 8008	$10.95
2650	8 Bit MPU	26.50
P8085	CPU	29.95

SR'S

2504	1024 Dynamic	$ 3.95
2518	Hex32 BIT	4.95
2519	Hex 40 BIT	4.00
2522	Dual 132 Bit SSR	2.95
2524	512 Dynamic	.99
2525	1024 Dynamic	2.95
2527	Dual 256BIT	2.95
2528	Dual 250 Bit Static	4.00
2529	Dual 512 BIT	4.00
2532	Quad 80BIT	2.95
2533	1024 Static	2.95
3341	Fifo	6.95
74LS670	16 x 4 Reg	1.95

UART'S

AY-5-1013	30K Baud	$ 5.95

ROM'S

2513(2140)	Char. Gen.-upper case	$ 9.95
2513(3021)	Char. Gen.-lower case	9.95
2516	Char. Gen.	10.95
MM5230	2048 BIT(512 x 4 on 256x8)	1.95

MM5262	2K x 1	Dynamic RAM	3 for 1.00

RAM'S

1101	256 x 1	Static	$ 1.49
2101	256 x 4	Static	5.95
2102	1024 x 1	Static	1.75
2107/5280	4096 x 1	Dynamic	4.95
2111	256 x 4	Static	6.95
TMS4044-45NL	4K	Static	14.95
7489	16 x 4	Static	1.75
8101	256 x 4	Static	5.95
8111	256 x 4	Static	6.95
8599	16 x 4	Static	3.49
21L02/91L02	1024 x 1	Static	1.95
74200	256 x 1	Static	6.95
93421	256 x 1	Static	2.95
MK4116(UPD416)	4K	Dynamic 16 Pin	5.95
MK4027(UPD414)	16K	Dynamic 16 Pin	29.95

PROMS

1702A	2048	Famos	$ 5.95
5203	2048	Famos	14.95
82S23	32 x 8	Open C	5.00
82S123	32 x 8	Tristate	5.00
74S287	1024	Static	7.95
3601	256 x 4	Fast	3.95
2708	8K	Eprom	10.95
2716 T.I.	16K	Eprom	29.95
2716 Intel	16K	Eprom	59.95
6301-1	1024	Tri-State Bipolar	3.49
6330-1	256	Open Collector Bipolar	2.95

SPECIAL REQUESTED ITEMS

FCM3817	$5.00	11C90	19.95	7205	19.95	9368	3.95
AY-3-8500-1	7.50	4N33	3.95	ICM7045	24.95	LD110/111	25.00/set
AY-5-9100	14.95	8T20	7.50	ICM7207	7.50	95H90	11.95
AY-5-9200	14.95	8T97	1.50	ICM7208	19.95	MC3061P	3.50
AY-5-9500	4.95	HD0165	7.95	ICM7209	7.50	MC4016 (74416)	7.50
AY-5-2376	14.95	MCM6571	13.50	MK50240	17.50	MC1408L7	4.95
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82S115	19.95	MCM6575	13.50	TIL308	10.50	74C922	9.95

CLOCK CHIPS

MM5309	$9.95
MM5311	4.95
MM5312	4.95
MM5314	4.95
MM5316	6.95
MM5318	9.95
MM5369	2.95
MM5841	9.95
CT7001	5.95

PARATRONICS

Featured on February's Front Cover of Popular Electronics

Logic Analyzer Kit Model 100A

$229.00/kit

Model 100A Model 10

- Analyzes any type of digital system
- Checks data rates in excess of 8 million words per second
- Trouble shoot TTL, CMOS, DTL, RTL, Schottky and MOS families
- Displays 16 logic states up to 8 digits wide
- See ones and zeros displayed on your CRT, octal or hexadecimal format
- Tests circuits under actual operating conditions
- Easy to assemble— comes with step-by-step construction manual which includes 80 pages on logic analyzer operation.

(Model 100A Manual - $4.95)

- Some applications are:
  - — Troubleshooting microprocessor address, instruction, and data flow
  - — Examine contents of ROMS
  - — Tracing operation of control logic
  - — Checking counter and shift register operation
  - — Monitoring I/O sequences
  - — Verifying proper system operations during testing

PARATRONICS TRIGGER EXPANDER - Model 10

Adds 16 additional bits. Provides digital delay and qualification of input clock and 24-bit trigger word. — Connects direct to Model 100A for integrated unit).

Model 10 Kit - $229.00
Baseplate — $9.95
Model 10 Manual — $4.95

B+K PRECISION 3½-Digit Portable DMM

- Overload Protected
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- DC Accuracy 1% typical

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AC Voltage: 0-1000V
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DC/AC Current: 0-100mA
Resistance 0-10 megohm
Size: 6.4" x 4.4" x 2"

Model 2800 $99.95

Comes with test leads, operating manual and spare fuse.

Accessories:

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CSC 100 MHz 8-Digit Counter

- 20 Hz-100 MHz Range
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Charger/Eliminator use 110 V AC — Model 100 — CAI $9.95

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(6" long X 4" wide)

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PB102 - 7" x 4.5"	39.95
PB103 - 9" x 6"	59.95
PB104 - 9.5" x 8"	79.95
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(includes power supply)

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DM1 - Circuit Designer $69.95
DM2 - Function Generator $74.95
DM3 - RC Bridge $74.95

LOGIC MONITOR for DTL, HTL, TTL or CMOS Devices **$74.95**

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QT type	#holes	price
QT-59S	590	12.50
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QT-47S	470	10.00
QT-47B	bus strip	2.25
QT-35S	350	8.50
QT-35B	bus strip	2.00
QT-18S	180	4.75
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The Pennywhistle 103 is capable of recording data to and from audio tape without critical speed requirements for the recorder and it is able to communicate directly with another modem and terminal for telephone "hamming" and communications for the deaf. In addition, it is free of critical adjustments and is built with non-precision, readily available parts.

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- **Maximum Data Rate** ....300 Baud.
- **Data Format** ....Asynchronous Serial (return to mark level required between each character).
- **Receive Channel Frequencies** ...2025 Hz for space; 2225 Hz for mark.
- **Transmit Channel Frequencies** ..Switch selectable: Low (normal) = 1070 space, 1270 mark; High = 025 space, 2225 mark.
- **Receive Sensitivity** ....−46 dbm accoustically coupled.
- **Transmit Level** ....−15 dbm nominal. Adjustable from −6 dbm to −20 dbm.
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- **Power Requirements** ....120 VAC, single phase, 10 Watts.
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Requires a VOM, Audio Oscillator, Frequency Counter and/or Oscilloscope to align.

The Original the 3rd Hand

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- *Leaves two hands free for working
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- *Position board on angle or flat position for soldering or clipping
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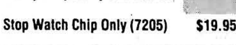
DIGITAL STOPWATCH

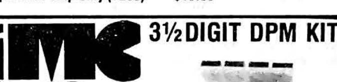
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- New Bipolar Unit
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- Single IC Unit

Model KB500 DPM Kit $49.00
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The JE700 is a low cost digital clock, but is a very high quality unit. The unit features a simulated walnut case with dimensions of 6" x 2½" x 1". It utilizes a MAN72 high brightness readout, and the MM5314 clock chip.

12 or 24 Hour

115 VAC **KIT ONLY $16.95**

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- 1 - 0
- ABCDEF
- Shift Key
- 2 Optional Keys

$10.95 each

New 63 KEY KEYBOARD

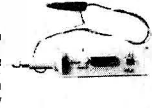
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This keyboard features 63 unencoded SPST keys, unattached to any kind of P.C.B. A very solid molded plastic 13" x 4" base suits most applications.

HD0165	Encoder Chip (encodes 16 Keys)	$7.95 ea.
AY-5-2376	Encoder Chip (encodes 88 Keys)	$14.95 ea.

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The Logic Probe is a unit which is for the most part indespensible in trouble shooting logic families TTL, DTL, RTL, CMOS. It derives the power it needs to operate directly off of the circuit under test, drawing a scant 10mA max. It uses a MAN3 readout to indicate any of the following states by these symbols (HI) - 1 (LOW) - 0 (PULSE) - P. The Probe can detect high frequency pulses to 45MHz. It can't be used at MOS levels or circuit damage will result.

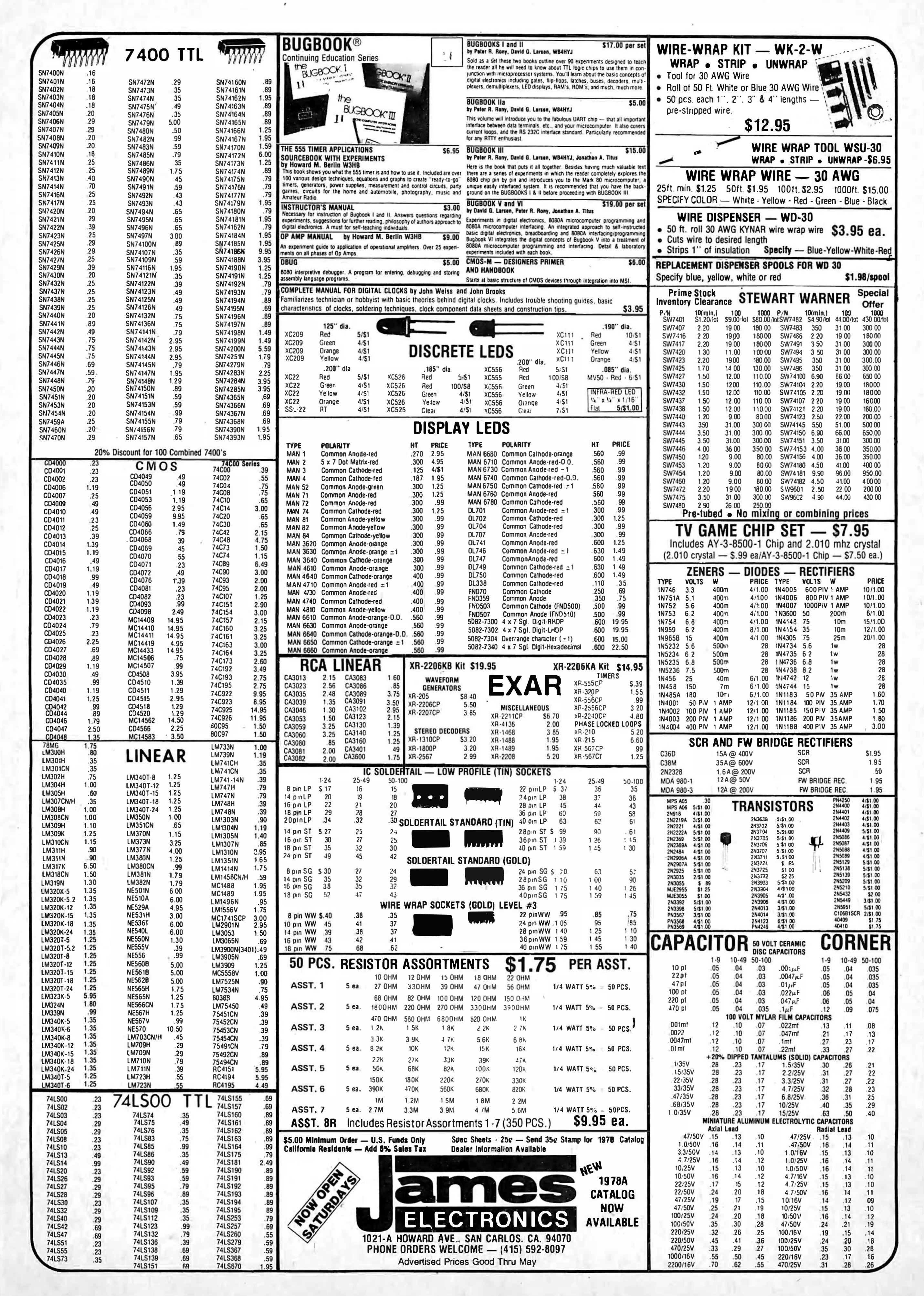


$9.95 Per Kit
printed circuit board

T²L 5V 1A Supply

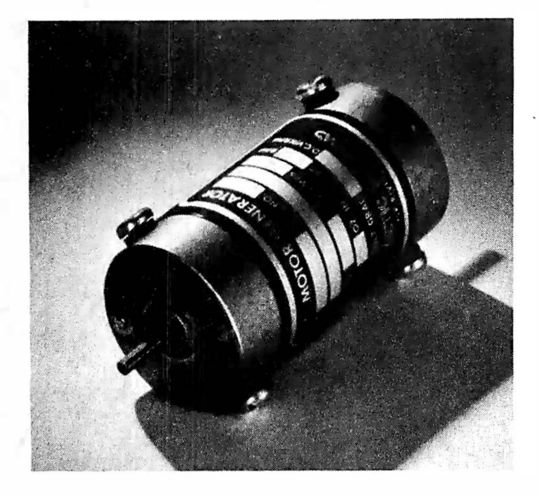


This is a standard TTL power supply using the well known LM309K regulator IC to provide a solid 1 AMP of current at 5 volts. We try to make things easy for you by providing everything you need in one package, including the hardware for only **JE225 $9.95 Per Kit**


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74LS40 .29
74LS42 .69
74LS47 .69
74LS51 .23
74LS55 .23
74LS73 .35
74LS74 .35
74LS75 .49
74LS76 .35
74LS83 .75
74LS85 .99
74LS86 .35
74LS90 .49
74LS92 .59
74LS93 .59
74LS95 .79
74LS96 .89
74LS107 .35
74LS109 .35
74LS112 .35
74LS123 .99
74LS132 .79
74LS136 .39
74LS138 .69
74LS139 .69
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Sold as a set these two books outline over 90 experiments designed to teach the reader all he will need to know about TTL logic chips to use them in conjunction with microprocessor systems. You'll learn about the basic concepts of digital electronics including gates, flip-flops, latches, buses, decoders, multiplexers, demultiplexers, LED displays, RAM's, ROM's, and much, much more.
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220/50V .45 .41 .36
470/25V .33 .29 .27
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2200/16V .70 .62 .55
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.47/50V .16 .14 .11
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What's New?

Precision Drive DC Motor

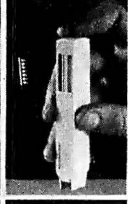


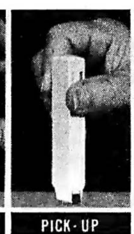
The MBG-150, a new DC motor and generator for precision drive applications such as tape cassette decks and medical and laboratory instruments, provides 1/30 horsepower, speed ranges of 1000 to 1, and load regulation of better than 1 percent. An optional feedback control system gives the unit more precise speed control and load regulation than is possible using variable voltage or silicon controlled rectifier approaches. Each rotor is dynamically balanced and test run for 24 hours prior to shipment. Typical MBG-150 design includes 24 VDC input with a speed of 6750 revolutions per minute at 5 oz-in continuous rated torque. Other designs are available as well from Dynetic Systems Inc, 19128 Industrial Blvd, Elk River MN 55330, (612) 441-4300.■

Circle 602 on inquiry card.

Straighten Pins and Insert Chips with This Tool







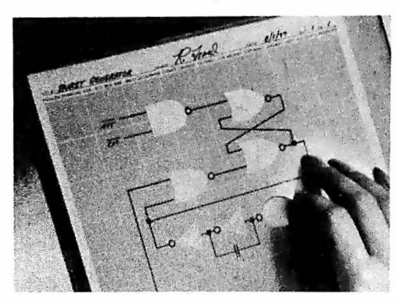


STRAIGHTEN PINS | RELEASE | PICK-UP | INSERT

The INS-1416 DIP Insertion Tool inserts 14 and 16 pin dual in line packages into sockets or predrilled boards. A pin straightener is built into the handle, with an automatic ejector from the straightening saddle. The insertion mechanism is designed to ensure accuracy, and the narrow profile of the handle permits it to be used on densely spaced circuit boards. The INS-1416 is $3.49 from OK Machine and Tool Corp, 3455 Conner St, Bronx NY 10475, (212) 994-6600.■

Circle 603 on inquiry card.

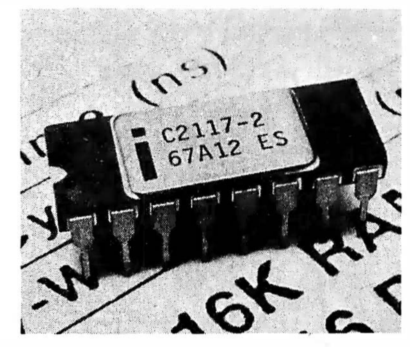
Thinking Aids for Logic Diagramming



This kit lets you construct logic diagrams by pressing plastic symbols on a special worksheet. Changes can be made simply by peeling off a symbol and moving it. The symbols stick to the worksheet electrostatically and require no adhesives. Following the latest ANSI standard, the symbols include ands, ors, amplifiers or buffers, delays, circles, blocks and rectangles. A starter kit (SKL-075), which comes with a padded vinyl folder, a set of ten 8.5 by 14 inch worksheets, a pad of 537 precut symbols, and a custom pen and eraser, is $10 plus $1.50 shipping from Fickled Thinking Aids, POB 6064, 990-M Enterprise St, Orange CA 92667, (714) 639-9061.■

Circle 604 on inquiry card.

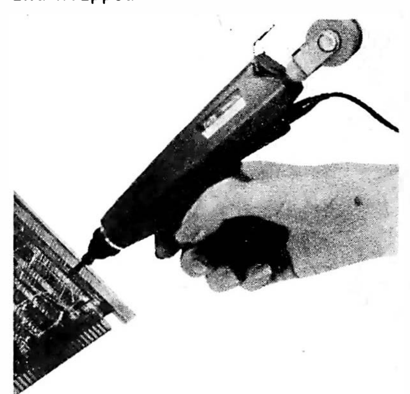
Second Generation 16 K Bit Memory Chip



The 2117 memory chip employs a fabrication process which has been used for nearly three years to produce the 2116 and other high density memory components. Its access time is as low as 150 ns. Power dissipation and maximum supply current have also been reduced, and the 2117 provides a 10% tolerance on all three power supplies, +5, +12 and −5 V. A new latched output mode can be used to provide hidden refresh, which does not disturb the chip's data output state. Prices in quantities of 100 or more range from $55 for the highest speed 2117-2 to $39 for the 2117-4 with 250 ns maximum access time, from Intel Corp, 3065 Bowers Av, Santa Clara CA 95051, (408) 249-8027.■

Circle 605 on inquiry card.

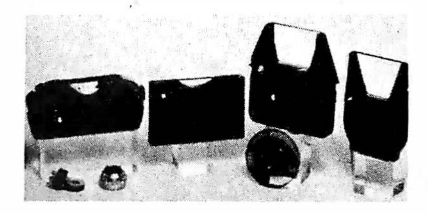
Now Standard Wire Can Be Slit and Wrapped



The new P184 Slit-n-Wrap bit makes it possible to wire wrap connections with standard 28 gauge Tefzel insulated wire without measuring, cutting and stripping. Previously only polyurethane-nylon wire could be slit and wrapped. The new tool can be used to "daisy chain" interconnections, avoiding the need to measure and cut the wire between each pair of wire wrap posts and requiring only about five seconds per post. A standard connection of seven wrapped turns has a resistance of only .003 ohms between post and wire and requires a force of more than ten pounds to pull it off. The Tefzel wire is available in 50 foot spools with red, green, white or yellow insulation, at a unit price of $4.18 per package of two 50 foot spools. The bit may be used with a Model P184-4T1 pistol grip wrapper with a 117 VAC motor ($89) or the Model P184-4T nickel cadmium battery powered pencil type unit ($80). A manual wrapper, the Model P184 ($29.50) is also available, from Vector Electronic Co Inc, 12460 Gladstone Av, Sylmar CA 91342, (213) 365-9661.■

Circle 606 on inquiry card.

Printing and Magnetic Media Supplies Offered in Small Quantities



Hobbyists can purchase small quantities of printing wheels, ribbons, diskettes, cassettes and other printing and magnetic recording supplies using Master Charge and VISA cards through this newly formed mail order source. The product lines offered include 3M Scotch and ITC Verbatim brand magnetic media, Qume and Diablo cartridges and printwheels, and IBM Selectric II compatible ribbons and typing elements. A catalog and price list may be obtained by writing Printcraft Systems Inc, Dept MO, 11-17 Beach St, New York NY 10013, (212) 966-0001.■

Circle 607 on inquiry card.

What's New?

Catalog Describes Micro Printer



This 14 page, four color brochure describes the AIP-40, a low cost ($425) 40 column alphanumeric impact printer. The AIP-40 includes a printhead, paper feed mechanism, power supply, and choice of serial or 8 bit parallel interfaces. The device prints at an average of 50 characters per second in a 64 character standard ASCII font. A serial interface can sustain a continuous 300 bps transmission and printing rate. The brochure, which details electrical and physical parameters, timing and character set, and suggested applications, is free from Datel Systems Inc, 1020 Turnpike St, Canton MA 02021, (617) 828-8000.■

Circle 579 on inquiry card.

First West Coast Computer Faire

The talks and technical papers presented at the First West Coast Computer Faire in San Francisco last April are now available in the form of a 320 page softbound book. The *Conference Proceedings* includes 93 papers under 25 topic headings, including computer art, speech synthesis and recognition, computers and music (43 pages), and the use of small computers in education (38 pages). Other sections provide both tutorial and design discussions concerning hardware and software for home computer systems. It is available for $12.68 ($13.40 for California residents) from The Computer Faire, POB 1579, Palo Alto CA 94305, (415) 851-7664.■

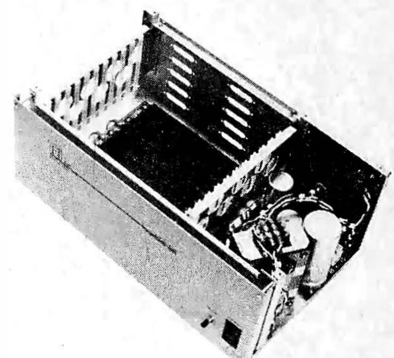
Circle 582 on inquiry card.

Report on Small Business Computers

All About Small Business Computers provides detailed specifications on 249 low cost computer systems for small business. Systems from 87 vendors are compared in 50 pages of comparison charts. Specifications covered include the minicomputer used in each system and its IO, mass storage and main memory features, keyboard and other IO facilities, communications capabilities, software support, pricing and availability. The report also summarizes the experience of about 750 survey respondents with a total of nearly 1800 minicomputers. Reprinted from *Datapro Reports on Minicomputers,* it is $12 per copy from Datapro Research Corp, 1805 Underwood Blvd, Delran NJ 08075.■

Circle 583 on inquiry card.

A Computer Needs a Foundation



Attention S-100 bus homebrewers: CMC Marketing, 5601 Bintliff, Suite 515, Houston TX 77036, is offering this foundation module manufactured by TEI Inc as the hardware basis of systems using one or more of the many Altair (S-100) bus boards available in the marketplace. According to the literature accompanying this photograph, the MCS-112 foundation unit contains a 12 slot mother board, along with a power supply rated at 17 A on the +8 V bus and 2 A on the −16 V and +16 V supplies. (With Altair (S-100) bus boards, regulators to produce typical +5 V, +12 V and −12 V are made a part of each board to transform the system supply voltages into locally usable voltages.) The heavy duty aluminum cabinet features a 115 CFM muffin fan which maintains positive pressure inside the cabinet, so that a washable dust filter can be used. The price of this hardware foundation for a homebrew system is $395. Also available is a larger chassis, model MCS-122 with 22 edge connector slots, and a power supply with 32 A at 8 V, 4 A at +16 V and 4 A at −16 V.■

Circle 581 on inquiry card.

An Important New Glossary

An interesting book entitled *Running Press Glossary of Computer Terms* has recently crossed our desk. The book is written by John Prenis, and is published by the Running Press, 38 South Nineteenth St, Philadelphia PA 19103. The book is available for $1.95 plus $.25 postage from the publisher, and we would expect it to be seen in numerous computer stores during the coming months.

There have been numerous glossaries published to date, to which the *Running Press Glossary of Computer Terms* is but the latest addition. However, there are several points to be made about this new glossary: it concentrates on a set of terms most likely to be encounterd by a new computer user trying to make sense of the field of computing for the first time.

Some samples of the definitions in this glossary, pulled from this 86 page paperback book, may provide the best way to illustrate what it can do for the reader:

Constant. Any number you don't expect to change. Instead of giving it a variable name, it can be written into the program explicitly. It's wise to make sure that you won't ever want to change it before you do this.

Data structure. The decision on how data are to be organized in memory and referred to by the computer is an important one. Picking the proper data structure can simplify the computer's job greatly. Some data structures often encountered are *files, lists, arrays, stacks,* and *queues.*

Matrix. A matrix is a two dimensional *array,* or table of numbers. In the hardware domain, a matrix can be anything arranged in a grid-like pattern.

Stack. The stack is a region of memory which works by special rules. Each time the computer stores a word there, it goes "on top of the stack," and all the previously stored words move down one level. When a computer takes a word off the top of the stack, everything moves up one level, until the stack is empty. Notice the computer has access only to the top of the stack. Piling a word on the stack is called a "push," and taking a word off is called a "pull" or a "pop." The stack simplifies some operations enormously.

User-oriented. Set up for somebody who is not expected to be knowledgeable about computers.

These definitions were picked "at random" to illustrate the typical terms and explanations found in the book, and illustrate the user-oriented nature of the terms. Engineering terms are for the most part omitted, unless they refer to the specification of a system's overall characteristics, and the majority of terms concern software concepts, which are the most important ones for a computer's users. As a starting point for the neophyte, this book of terminology is highly recommended. . .CH■

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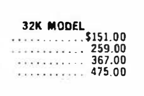
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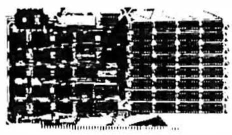
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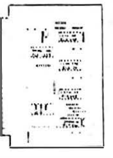
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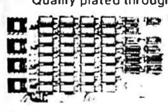
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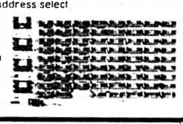
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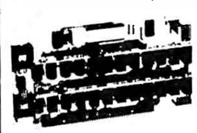
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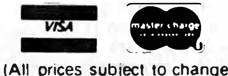
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Unclassified Ads

WANTED: For Microdata 1600 processor (Reality): magnetic tape controller and disk controller. Jack Hardman, 140 Forest Av, Glen Ridge NJ 07028, (201) 429-8880.

FOR SALE: Homebrew 8080, IMSAI front panel mounted in vector rack with 12 slot Altair (S-100) backplane and 15 A power supply, $450. 16 by 64 alphanumeric video display board, memory mapped with ASCII keyboard port, $100. 8 K memory, 450 ns, $150. 4 K memory, 450 ns, $75. Doug Lehmann, 1146 Scott St, Maumee OH 43537.

HEATH H9 VIDEO TERMINAL: Fully assembled and tested by an experienced engineer. Interfaces to virtually all microcomputer systems via RS-232, 20 mA loop or TTL. Includes many unique features. Price includes shipping. $530. R Edison, 4 Longfellow Pl, Boston MA 02114, (617) 742-3074.

FOR SALE: One Hewlett-Packard 2640A interactive display terminal, one Spintronic data communication terminal and one 3M dry photocopier. Purchased 1976 but hardly used due to illness. Original purchase price over $8000. Part of estate, will sell for $3000. George Danek, 1021 Harbor Dr, Rt 7, Annapolis MD 21403, (301) 263-3134.

WANTED: Hardware and software required to organize and maintain a mailing list. Please write if you have any information that can help me get this going. Write W Pomeroy, 5790 Bull Hill, LaFayette NY 13084.

WANTED: Used KIM-1 microprocessor. Prefer complete system with expansion boards if possible. Norman G Church, 18310 Franklin Way, Gladstone OR 97027, (503) 659-6763.

FOR SALE: Improved Sphere System 330. Consisting of 20 K dynamic memory, 2 K 2102s, 2 K EROM monitor, KC cassette interface, serial interface and 6830 modem chip, sockets for 8 K 2708s also with CRT interface, keyboard, and mother board. Requires only power supply and modified television. Only $700 takes this and more. Bill Vodall, Box 75, Kevin MT 59454, (406) 337-2222.

FOR SALE: Monroe programmable calculator Model 1830. Excellent condition, under factory service contract. Cost new $3100. Will sell for $2200, which includes about $800 worth of magnetic storage cards. B Fremerman, 4041 Central, Kansas City MO 64111.

FOR SALE: IBM 1620 system, $2000. Includes all software and curriculum materials that were used by the Mathematics Dept at Monona Grove High School. Donald Helstad, Principal, Monona Grove High School, 4400 Monona Dr, Monona WI 53716, (608) 222-1291.

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Please note that it may take three or four months for an ad to appear in the magazine.■

FOR SALE: Heathkit H9 video terminal assembled and tested. Used only 5 hours. $500. Howard Schimmelpfennig, 351 N 4th West, Logan UT 84321, (801) 752-1987.

FOR SALE: SwTPC 6800 computer system. KBD-3, TVT-II with modulator, AC-30, 8 K, interface cards, two recorders, software. Beautiful custom cases. Packaged for portability, $650. Anderson-Jacobson 841 Selectronic terminal. Correspondence code, RS-232 interface, modem and coupler. Attractive case. $725. Daniel L Wright, 280 Perrymont Av, San Jose CA 95125, (408) 925-3367 days.

FOR SALE: Teletype Model 35 ASR, heavy duty printer with paper tape reader/punch. Currently operating on 20 mA loop, convertible to EIA RS232. Has remote tape reader switch for use as local console or remote terminal. Best offer. Brad Jude, 428 Ridge Av, Clarendon Hills IL 60514, (312) 323-8093.

WANTED: Altair 8800 or 680 construction package with PC board etching guide and parts placement guide. Ben Galewsky, 1035 Dowlen Rd, Beaumont TX 77706.

FOR SALE: Altair 8800 minicomputer with 21 K programmable memory, 2 K read only memory, cassette interface, video display interface, parallel and serial IO interface, ASCII keyboard, video monitor, connecting cables, manuals and some software. Asking $1275. M Harris, POB 1053, New Britain CT 06050, (203) 225-0504.

WANTED: BYTE #7, volume 1, March 1976. Will trade volume 1, issues 1, 2 or 3 or cash. Write details. S Finberg, POB 82, MIT Br, Cambridge MA 02139.

REWARD: $10 for information leading to the comprehension of a Prentice P103 ANS modem. Need schematics, manual, etc. William L Palya, St Joseph's College, Rensselaer IN 47978.

FOR SALE: Computer Automation Alpha LSI 2/20G minicomputer. 16 bit processor, hardware multiply/divide, stack and byte processing, priority interrupts, DMA, read only memory automatic load, Teletype interface, 8 K core memory, power supplies, chassis, programmer's console. Includes general and interfacing manuals, partial schematics, software listings for: assemblers, diagnostics, editor, loaders and math functions. $1200 plus shipping, or trade for DEC LSI-11 equipment or 24 by 80 CRT. Paul Sorenson, 220 Cedar St, Apt 7, E Lansing MI 48823, (517) 337-0223 or 353-9487.

WANTED: Programs on 8 inch ICOM 3700 disk subsystem. I use ICOM-58, DE88I/IMSAI and FDOS 111. I also use the Cromemco Dazzler and the Cybernetic Speech Synthesizer. Please send me a copy of your disk and I will pay you for it. Dr John M Larimer, 55 La Gorce Cir, Miami Beach FL 33141.

FOR SALE: Assembled 8080 system, IMSAI 22 slot mother board, large power supply, PIC-8 28 K Godbout programmable memory, North Star disk, PolyMorphic video board, and Digital Group keyboard and cabinet, $2800. Morrow cassette board assembled, $70. Godbout read only memory with 4 K of 8080 assembler/monitor, $200. 3P+S kit, $110. Oliver tape reader assembled, $60. C Watrobinski, 4923 N Kedvale, Chicago IL 60630, (312) 736-6920.

FOR SALE: Make offer for complete set of BYTES, September 1975 thru October 1977, like new condition, sold singly or complete set to best offer. M Bakke, 448 Carlyle E, Belleville IL 62221, (618) 235-5686.

FOR SALE: Digital Group Phi Deck digital tape system (6400 bps), 20 second access time. Four drive cable case controller board. All factory assembled and tested. Used for three months, working fine when replaced by disks. All documentation and Phi-Mon operating system. Asking $624, you save $136. Will consider trades; I need a sophisticated terminal. Will ship UPS collect upon confirmation and receipt of $60 deposit. Confirm by phone (804) 838-1950 Monday thru Friday 8 AM to 5 PM.

FOR SALE: Five 4 K Altair (S-100) static memory boards. Factory assembled and still on warranty, one never out of box. I am switching to 16 K boards. $100 each. No cash please. Al Marshall, 408 Oakwood, Angola IN 46703.

FOR SALE: ASR 33 Teletype, new covers, working reproducing tapes now, on stand and with plywood shipping crate, used, $650. Teletype 1 inch paper tape $4 per 7 roll box. Altair 680b ready to go, $375. Digideck digital Philips cartridge tape deck and electronics, all documentation, $145. These tape decks look perfect but are untested. All items plus shipping. Jim Beistle, 3728 Wilkie Way, Ft Worth TX 76133.

WANTED: BYTE volume 1, issues 1 thru 11. Must be in good condition. Mail price to Byron de Vries, Box S-281, Castle Point Sta, Hoboken NJ 07030.

LINE PRINTER: Altair 88LP Okidata 110 with tractor feed, controller, cable and documentation for sale. Less than one roll of paper run through it. Cost new $1750, will sell for $1400; you pay freight. Dave Uhring, 710 Cedar St, Collinsville IL 62234, (618) 344-5188 days.

FOR SALE: Altair (S-100) microcomputer, assembled and tested. 8080 processor, VDM-1 video display, Solid State TV monitor, Tarbell cassette, Pennys recorder, ASCII keyboard, Tarbell disk controller with Cal Comp 140 disk, CPM software, 44 K static memory, parallel IO board with two inports, two outports, 12 position mother board, 28 A power supply and cabinet. Comes complete with popular software, all ICs socketed, and full documentation, $3000. P. Sargent, 4209 Knoxville, Lakewood CA 90713, (213) 421-9521.

FOR SALE: Complete PolyMorphic system, includes processor board, two 8 K boards, video board, 5 slot mother board, Panasonic tape recorder, keyboard, converted TV, all cables and assorted prerecorded software. All less than 9 months old, preassembled. Valued at over $2300, will sell to best offer over $1750. Scott Hayden, 23921 Colfax St, Lowell IN 46356, (219) 552-0232.

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FOR SALE: IMSAI 16 K assembled memory certified good by IMSAI: $299. Assembled and tested Poly 88 System 2: $499. Assembled and tested (virtually new) IMSAI disk drive with interface, cable, and DOS-A (FDC2-1, FIF, Cable C, DOS-A): $1399. Shipping paid. Call Greg Jewell to reserve the equipment you want. (208) 234-0495 evenings.

FOR SALE: CT1024 socketed, RS232 interface, good condition, $95. Les Zoltan, 151 Buckingham Dr #280, Santa Clara CA 95050, (408) 984-7698.

FOR SALE: Hewlett-Packard Model 1601A logic state analyzer for use with any 180 series mainframe as a display unit. Includes two Model 10231A 6 bit data probes, and two blue light filters — one for 182 and one for 180 series display units. See HP 1976 catalogue, page 82, for further info. Brand new condition, $1400 or best offer. Mike Rosenthal, 906 NW 30th St, Corvallis OR 97330, (503) 754-0593 evenings.

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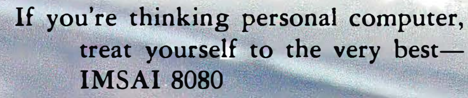
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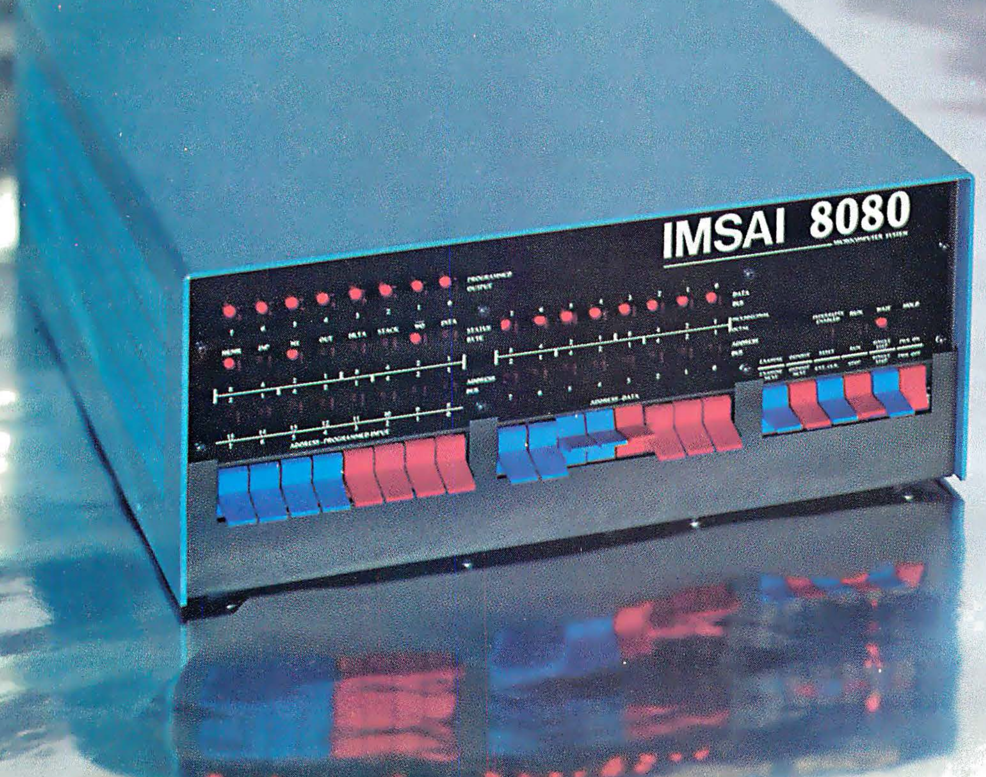


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